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TECHNICAL REPORT NO. 13

BRLESC I DISC SYSTEM

by

Gordon L. Herald

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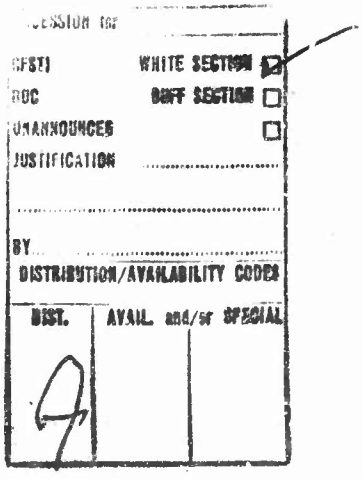

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JANUARY 1972

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Gordon L. Herald

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A B E R D E E N P R O V I N G G R O U N D , M A R Y L A N D

A B E R D E E N R E S E A R C H A N D D E V E L O P M E N T C E N T E R

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I. INTRODUCTION

In September of 1971 two Bryant 1100 disc drives were placed on-line for users of the BRLESC I computer. Each disc drive unit is capable of storing about 812,000 BRLESC words. A portion of the first disc contains the compilers, subroutines and FORTRAN programs. The remainder is available to the programmer for use as temporary storage. The second disc drive unit is available to the programmer for temporary storage or to mount the programmers disc pack. In the event that a program requires three disc drives, provisions have been made to connect a BRLESC II disc drive to BRLESC I.

Although the BRLESC I is scheduled to be replaced by the acquisition of a large commercial computing system, BRLESC II will be retained. Currently, BRLESC I and BRLESC II each have two disc drives. Six months after the commercial system becomes operational the two disc drives currently assigned to BRLESC I and described in this report will be assigned to BRLESC II thereby doubling the capacity of immediate access storage on BRLESC II.

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II. THE BRYANT 1100 AND IBM 2311 DISC DRIVES

The disc packs used on the BRLESC I and II disc drives have 12 surfaces, 10 of which are available for data storage. Each surface has 203 tracks for a total of 2030 tracks. The track capacity is approximately 400 BRLESC words.[1] The disc drives provide 10 read/write heads (1 for each surface) fixed to a common carriage assembly (see fig. 1). Track access is achieved both mechanically and electrically. Any one of a group of ten tracks can be accessed by electronically selecting one of ten read/write heads. To access any other group of 10 tracks the head assembly must be mechanically repositioned.

Repositioning the heads from cylinder zero to cylinder 202 requires a maximum of 135 milliseconds.[2] Cylinder to cylinder repositioning requires 25 milliseconds. Once the heads are positioned and a read or write command is initiated there is an average delay of 12.5 milliseconds (average rotational delay at 2400 rpm) until the index point is sensed at which time data transfer begins.

Disc rotation causes a thin film of air to exist at the surface which permits the read/write head to float at a height of 125 to 160 microinches from the surface. If the heads are allowed to crash into the disc surface damage may result to the track such that it may be unusable for storage. For this reason the disc drives and the controller have been designed so that the heads are retracted before the drive motor is shut down.

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1. BRLESC words are 72 bits.
2. The cylinder concept is defined as that imaginary surface which can be accessed by the 10 read/write heads without moving the carriage.

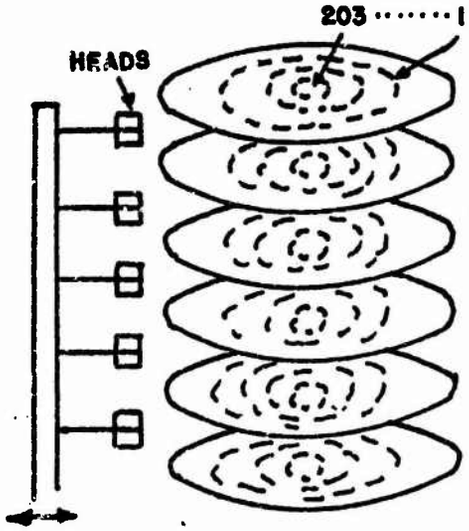


Figure 1

A single head is used for both reading and writing and consequently does not allow for a read after write check as is done on the tape transports. Double frequency non-return-to-zero (NRZ) recording is used. Double frequency recording is the term given to a recording system that puts a clock pulse at the beginning of each bit cell time. In the NRZ recording system each transition of magnetization from plus to minus or minus to plus represents a bit (see fig. 2).

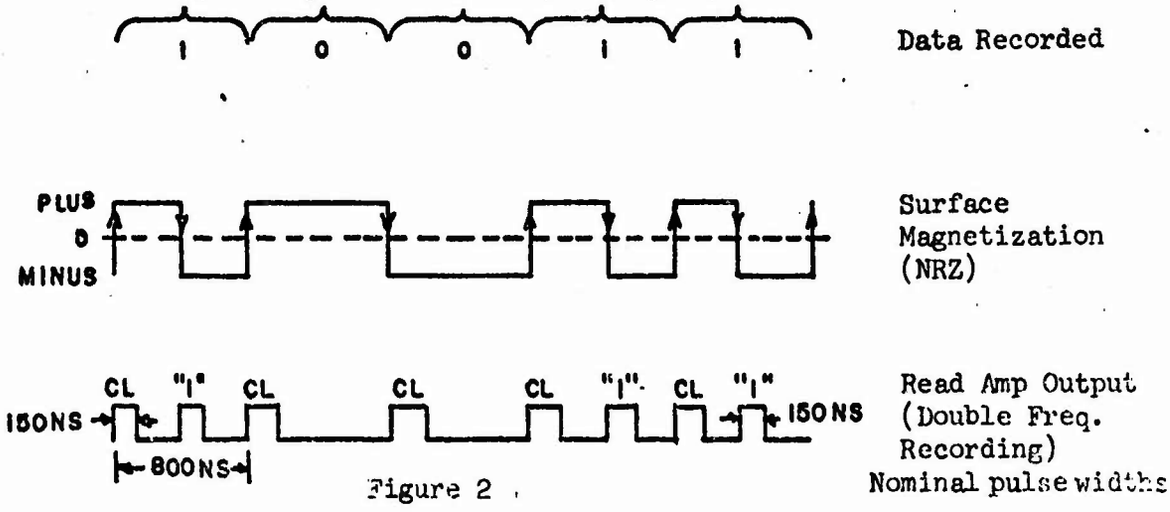


Figure 2

Each read/write head has an erase head, however, this erase head does not erase across the entire width of the track. Also, the erase head is behind the read/write head, therefore, there is no erase prior to writing. The erase head does nothing more than erase the outer edges of the recorded track to provide a .005 inch recorded track width, thus providing physical separation between adjacent tracks and reduction of noise pickup by the read head from adjacent tracks.

III. DISC CONTROLLER

The disc controller is attached to the ½" tape I/O control in X-row and operates as unit "0". This conflicts with the typewriter which is also unit "0", however, IR bit 15 distinguishes tape and typewriter orders from disc orders. The disc can be operated on either trunk A or trunk B. Since the discs will be daisy chained they cannot be operated concurrently on separate trunks. Tape Move Forward B Blocks order plus IR 15 will cause a Set Disc Address order to be executed by the disc. The required IAS is determined by instruction register bits 41-60. IR bits 55 and 56 select one of four disc units, bits 45 through 52 select the cylinder, and bits 41 through 44 select the head. An example of a Set Disc Address order is: ø8(ØØ754)ØØØØØ)ø42ø3). This order selects the ØØ disc (discs are designated ØØ, ø1, ø2, ø3), cylinder 75_{16} (117_{10}), head 4, trunk A (Cγ portion specifies trunk). Heads are designated ø-9, and cylinders are designated ø-NK. An Address Error will occur if a head address greater than 9 is specified or a cylinder greater than NK.

Disc read and write operations are in either the 8x64 or 8x72 bit mode.[1] Disc Read or Disc Write commands will commence at the disc unit, cylinder, and head locations last specified in a Set Disc Address order. An example of a disc write order is: ø8(ØØ1ØØ)ØØØ1N)ø61øK). This order writes 1N words starting from location 1ØØ, using 72 bit words, trunk A. An example of a disc read order is: ø8(ØØ2ØØ)ØØØ1N)ø6ØØ5). This order reads 1N words starting at location 2ØØ, using 64 bit words, trunk B. See Table I for disc orders.

---

1. 8x64 = 8 bits/character 64 bits/word
   8x72 = 8 bits/character 72 bits/word

IV. SPECIAL X-ROW CIRCUITS IN BRLESC I
(Reference-I/O Control Book 600)

Special circuits have been added to the $\frac{1}{2}$"tape system in X-Row to accomodate the disc. I/O control book p. 605 has an added FF(pack 2) and buffer to provide a disc error halt indicator and also to provide a signal via pin 35 to generate Abnormal Halt. Page 606 and 607 have an additional gate (pack 3) to decode the disc Error Halt. Page 612 and 613 have circuits which provide the Disc Order, Set Disc Address (SDA) and Gate Disc Address (Gate DA) Signals. This is the point at which disc orders are distinguished from tape orders. An additional gate (pack 22) has been added on page 616 to provide detection for a Units "0" Conflict in the case where disc orders would be stacked on both trunks. Pages 606 and 607 have SDA to 18,2 which will prevent an Equality Clear and a Release Buffer (at ∅7-2). This will occur because bits 21-40 will normally be zero in the ∅8 disc order and cause IAS=FAS. Additional logic (packs 3, 4, 5, 10) have been added to page 617 to distinguish between a unit "0" typewriter order and disc order. The $\overline{\text{Units "0" Conflict}}$ signal is also developed so that typewriter and disc are permitted to operate concurrently. SDA has been added to gates 14,6 and 20,2 (see p. 634) to inhibit LOW during a Set Disc Address. During SDA (the IAS is being used for disc addressing) there is no memory data transfer and it is desirable to inhibit LOW to permit concurrent control and arithmetic operation during this time. Page 638 is the logic provided to enable 20 bits of the IAS to be used as disc addresses.

V. CONTROLLER OPERATION - Set Disc Address (SDA)
(Reference SDA Timing and Disc Logic)

To enable selection of a disc module, head, and cylinder the controller uses the disc address (DA) bits from X-row. DA bits 15 and 16 will select one of four disc modules. Once the module is selected one set of flip-flops will store the present disc cylinder address from the selected disc module, a second set of flip-flops will store the new cylinder address from X-row, and a third set of lip-flops will store the head address from X-row. The flip-flops are located on the difference boards (D5, D6, D7). The difference boards will then send to the disc the new cylinder address which will become the present disc address on the next SDA order. As these operations are occurring the difference boards will determine the difference between the present cylinder address and the new cylinder address and the direction of movement (forward or reverse). Next the new head address is sent to the disc module along with the direction of movement. Finally the difference is sent to the disc module which then advances or retreats the specified number of cylinders. During SDA operation the controller will generate a Release Buffer and BRLESC I cannot reaquire the disc until Gated Attention from the disc module is reestablished at the completion of the SDA. Sequencing of function commands to the disc module is provided by board D4. SDA control is provided by board D21.

VI. SET DISC ADDRESS - Detailed Discussion

The I/O Control in BRLESC I will send signals C1 through C6 and the 14 DA bits to the controller. The decoder board (D1) will decode C1 through C6 and generate the Initiate SDA pulse to be sent to SDA control (D21). First a Clear Module Select pulse (D21,5) is formed to clear the Module Select Flip-flops on D22. The SDA Control sequencer (S1, S2, S3, S4) is started and S1 allows setting of the desired disc module via pins 10, 11, 12, or 13 as selected from the module decoder formed by packs 13, 18, 24, 25. One of four MOD SEL outputs from board D22 will be sent to the disc via driver board D8. The selected disc will return a MOD signal to board D15 where a check occurs between the MOD SEL and SEL MOD signals to insure that the requested disc has been selected. The checking circuit then forms the MOD SEL OK signal which enters the SDA Control at D21,20 and enables the CLEAR ADDRESS, SET ADDRESS, and DIFFERENCE STROBE in that order. CLEAR ADDRESS is sent to D5,40; D6,40; and D7,40 to clear the head address registers and the present and new cylinder address registers. SET ADDRESS will set the present cylinder address and the new cylinder and head address from X-row into the flip-flops on D5, D6, D7. SET ADDRESS to D4,10 starts the function command sequencer A', B', C', D', E' on D4 and also disables READY at D20,6 to D1, 20.

The controller takes the old CAR addresses (Bj) and the new CAR addresses (Aj) and computes the difference and direction that the read/write heads are to move. The disc drive requires the complement of the difference. The controller difference boards in D5, D6, D7, generate $\bar{D}$ (difference complement) which can be stated as:

$$\bar{D}j = AjBjCj + \bar{A}j\bar{B}jCj + Aj\bar{B}j\bar{C}j + \bar{A}j\ Bj\ \bar{C}j$$

The carry terms are given as:

$$Cj_{+1} = AjBjCj + \bar{A}j\bar{B}jCj + XAj\bar{B}j + \bar{X}AjBj$$

(X = true if $A \geq B$)

If A ≥ B then the final C_{out} is positive. If A < B the final C_{out} is negative, X becomes true (refer to flip-flop 12 on D21) and new difference results are generated and sent to the disc drive. The difference strobe (D21,17) checks for A < B condition and sets the forward/reverse flip-flop. X on the logic prints is equivalent to Y (reverse); thus in cases where A < B (X = true) the disc drive will move the read/write heads backwards.

When A' of the function command sequencer is up CONTROL (D4,38) and FILE BUS (D6,35) will cause the head registers in the selected disc to be reset. B'will generate SET CYLINDER (D4,37) and this plus the appropriate file bus lines on D5, D6, D7 will cause the cylinder address register in the selected disc to be set. C' on D4,33 (SET HEAD) and the appropriate file bus lines will set the head address registers and direction of head carriage movement of the selected disc and also release the I/O Control in BRLESC I by generating a RELEASE BUFFER signal. D' on D4,35, (SET DIFFERENCE) and the appropriate file bus lines on D5, D6, D7 will send the difference results to the selected disc. At E' time the controller will again generate CONTROL at D4,38 and enable FILE BUS 2 to cause the disc to seek the new address. When the disc has completed the seek operation GATED ATTENTION will be returned to D20 to enable READY so that I/O Control can acquire the disc controller for the next command.

VII. CONTROLLER OPERATION - Write
(Reference-Disc write timing, CRC timing and Disc Logic)

The write command from the I/O Control can specify writing of 72 bit or 64 bit words. The track capacity is 400 - 72 bit words or 450 - 64 bit words. The controller utilizes double buffering to transfer data from the I/O Control to the disc controller. There are two 8-bit data registers. Eight bit register A receives data sent serially from the I/O Control while 8-bit register B is serially shifting data to the disc. Next register B will receive data from the I/O Control while register A shifts data to the disc. A CRC register is associated with each data register. Track format is compatible with BRLESC II and the Hybrid machine. Starting from the index position on the track there will be recorded 162 initial zeros, 2 initial ones, 28,800 data bits, an 8-bit CRC1, and 8-bit CRC2, and a final clock. The disc controller always writes 28,800 data bits even if the I/O Control has specified a lesser number. When the I/O Control specifies less than 28,800 data bits the disc controller will automatically write zeros until 28,800 data bits have been written.

VIII. WRITE - Detailed Discussion

The I/O Control in BRLESC I will send signals C1 through C6 to the decoder board D1 which will decode and generate PREPARE TO WRITE (D1,38) and, after a .6us delay to enable checking for illegal write, INITIATE WRITE (D1,36). Refer to D14 and note that INITIATE WRITE will set ERASE FF (D14,25) and, after the index pulse is received, INDEX FF. The following clock will set the WRITE FF and the WRITE INITIAL "0" FF and provide the WRITE INITIAL ZEROS (D14,5) output to enable the COUNT (D14,12) to the counter (D10), COUNT 162(D9,28) and RESET COUNT (D9,5) after 163 clocks. COUNT 162 sets the WRITE INITIAL "1"s FF on D14 which permits writing of two initial 1's following the 162 initial zeros. Approximately 400 ns after a count of 163 clocks, RESET COUNT (D9,5) will toggle the Initial "1"'s flip-flop which in turn toggles the Write Data flip-flop and provides WRITE DATA F.F. (D14,40) to enable WRITE CLKS INTERFACE (D14,11) and WRITE DATA CLOCKS (D14,16).

During the write initial zeros time period, data from X-row is being transferred to the two 8-bit data registers. INITIATE WRITE, TAG CLOCK, and C8 (count 128) generates START DATA XFER (D12,6) to D2,34. Refer to D2 and assume writing of 72-bit words. Gate 12,10 will generate two pulses (INITIAL START BURST) under control of flip-flops 11 and 16. The trailing edge of each pulse will allow the burst generator (packs 2, 3, 4, 5, 8, 9, and 50 ns delay line) to send a burst of eight pulses (D2,5) to the 72-bit register in X-row. Eight data bits will be entered in 8-bit register A via 5, 13 and 4, 13 on D16. The Select Register FF on D16 will be toggled by TOGGLE SEL REG FF (D2,18) so that the next eight data bits will enter register B. The Select Reg. FF is again toggled from D2,18. Both 8-bit registers are now filled and when WRITE DATA CLOCK is presented to D16,10 data will be shifted off A register to the disc under control of bit counter on D16 formed by packs 11, 12, 13, 14 and 7. After eight bits have been shifted off register A gate 7,10 on D16 will toggle the Select Register FF and

allow data to be shifted off register B to the disc. Simultaneously the START BURST (D16,7) pulse will start the burst generator on D2 and data from X-row will be transferred to 8-bit register A. Data transfer from X-row will alternately be entered into register A and B and data shifted to the disc will alternately be shifted from register A and B. After 28,800 bits have been recorded Reset Control will generate RESET COUNT (D9,5) which will reset the Write Data FF on D14 and set WRITE CRC FF (D14,15). Pack 24 will toggle and allow RESET COUNT to generate DATA CLEAR (D14,41) and SET CRC (D14,42) on the following clock. These signals enable clearing of both 8-bit data registers and transfer of the CRC register contents to the data registers. WRITE CRC FF to D16,19 enables WRITE DATA CLOCK to transfer the contents of the 8-bit registers, which now contain the CRC, to the disc. After the last of 16 CRC bits are transferred to the disc one more clock is written and count C5 sets Reset Write FF which will reset the Write CRC FF and inhibit gate 12,10 to stop write clocks. A count of 97 is allowed before RESET WRITE FF to D9,30 generates RESET COUNT to D14,30 to toggle pack 19 on D14 which brings up WRITE RESET (D14,18) to D9,20 and generates the 500-600 ns RESET pulse (D9,40) which resets ERASE FF (D14,25) and terminates the write operation by generating a RELEASE BUFFER at D20,40 to X-row.

Disc writing may also be performed in the 64-bit per word mode. Two INITIAL START BURST pulses are generated as in the 72-bit mode, however, the burst triggered at the trailing edge of the first INITIAL START BURST pulse is a dummy shift used to shift and discard bits 65 to 72 off the 72-bit register in X-row. ENABLE DATA Reg. (D2,40) to D16,40 will prevent the 8-bit dummy shift from entering the 8-bit registers. COUNT EOW (D2,26) pulse is permitted, however 16,13 is still negative and inhibits the TOGGLE SEL REG FF (D2,18) so that the next burst will still enter 8-bit register A. After the second INITIAL START BURST pulse 16,13 will be positive and permit ENABLE DATA REG (D2,40) to D16,40 and TOGGLE SEL REG FF (D2,18) to D16,18. Flip-flop 13,13 on D2

will be set positive by 14,13. At the end of the second 8-bit burst 17,10 will go positive and packs 15, 17, 10 and 1.2 us delay will form a 1.2 us pulse at 10,9 and 19,14 to reset flip-flop 13,13 and the burst generator to generate a third burst to shift data to 8-bit register B. The EOW pulse at the end of each word resets 13,13 positive so that the START BURST pulse (D2,7) provides the 8-bit dummy shift and 13,13 enables the START SPECIAL BURST at 19,14.

Flip-flop pack 6 on D16 is used to gate the TOGGLE SEL REG FF (D16,18) and START BURST (D16,7) pulse. TOGGLE SEL REG FF pulse is only utilized when preparing to write the first word.

IX. CONTROLLER OPERATION - Read
(Reference-Disc Read Timing and Disc Logic)

Disc reading is permitted in either 64 or 72-bit words. Double buffering, using two 8-bit registers, transfers data serially from disc to I/O Control. The disc controller begins searching for 97 consecutive zeros after the index position is sensed. Next it will search for the two initial ones. This procedure insures that data will immediately follow the initial ones. Reading of data procedes until a count of 28,800 data bits occurs, then the two 8-bit CRC characters are read and a CRC error strobe is generated, followed by a release buffer to I/O Control. CRC errors are normally ignored since software has data checking provisions.

X. READ - Detailed Discussion

The I/O Control will send signals C1 through C6 to the decoder board D1 which will provide INITATE READ (D1,37) to D13,3. The trailing edge of the index pulse from the disc will set READ FF (D13,30) and READ INIT. ZEROS (D13,26) positive. READ FF to D4,16 and D7,28 enables pulse shaping logic formed by packs 17, 18, and 19. If 12,10 of the Clock/Data FF is positive a READ CLOCK (D13,16) pulse is sent to D12,15 where it will be changed to a 100 ns pulse and started down a 1 us delay line. At 600 ns INFO STROBE (D13,43) will enable 24,13 and 22,9 for 100ns to form READ COUNT (D13,18) and COUNT (D14,12). After 97 initial zeros are counted RESET COUNT (D9,5) is generated and Read Zeros FF (D13) is reset which causes Init. Ones FF to be set. At this time the counter has been cleared and, since READ INIT. ZEROS (D13,26) is negative, no further counts are permitted. Ones from the disc will set info flip-flop (pack 23 on D13) so that INFO STROBE will enable a 100 ns pulse at 24,14 to 5,6. After two initial ones occur, READ DATA FF (D13,27) will be set. The controller is now set to read data from the disc and transfer it to the 8-bit registers from D13,36 and D13,19 to D16,32 and D16,34 respectively.

Attention now shifts to the Register Control board D16. INITIATE READ (D16,37) gates the "1" and "0" data bits to the A or B 8-bit register as selected by the Select Register flip-flop. After eight data bits have entered the registers, bit counters formed by pack 11, 12, 13 and 7 on D16 will generate a CHANGE REG. pulse at 7,10 and START BURST (D16,7) pulse whose trailing edge will trigger the burst generator on D2 and shift data to I/O Control. The CHANGE REG pulse toggles the Sel. Reg. FF so that data from the disc now enters the 2nd 8-bit register while data is being shifted to I/O Control from the first. Alternating of 8-bit registers continues through the entire read operation. After 28,800 data bits have been read a RESET COUNT (D9,5) will be sent to

D13,25 and set READ CRC FF (D13,10) and reset, after a count of 2, READ DATA FF (D13,27). Data to I/O Control is now inhibited, however, the CRC characters are shifted into the 8-bit registers to be added to the CRC registers by means of logic packs 17, 22, and 24. If no read errors occurred the CRC registers will now be zero. After the 16 CRC bits have been transfered to the 8-bit registers, counter stage C5 at D13,11 will generate a CRC ERROR STROBE (delayed by .5us to allow the CRC add to be completed). CRC ERROR STROBE fires a one-shot which will generate READ RESET (D13,35) to D8,41 and cause RESET (D8,40) to D20,26 which will provide RELEASE BUFFER (D20,40) and terminate the read operation.

XI. CONTROLLER OPERATION - Power Sequencer (Reference-Disc Logic)

The power sequencer enables the DC and three phase AC power to the disc units when sense circuits determine that all DC supplies are on and at their sepcified voltages. Packs 1,3; 6,6; and 11,4 on D24 will provide negative outputs if the +6, +3, +4.5, -2, and -36 volt supplies are operational. Pack 6,4 will provide a positive output if the -3V supply is operational. When all DC supplies are operational gates 3,14 and 7,10 will be at logic "1". Momentarily depressing the NORMAL ON pushbutton will now enable 3,10 to operate relay R1 and switch DC to the discs. Pulse circuit (packs 5,24, 19 and 7) set a delayed single shot (25ms) which sets JK flip-flop 14,13 and operates R3 which operates R4 and switches three phase AC to the discs. The +36 volt supply in the disc is now on and is sensed by the controller D24,29. This enables R2 to latch up and remove ground from 4,1 and provide CONTROLLED GROUND (D24,36) to the discs. Gate 9,13 goes positive and permits gate 3,10 to latch. CONTROLLED GROUND enables the heads to extend. Sensing of HEADS EXTENDED (D24,15) results in gate 4,9 becoming positive thus maintaining the latch on 3,10.

NORMAL OFF releases R2 and breaks CONTROLLED GROUND to the discs. Gate 9,13 will go negative, however, 4,9 will remain positive until the heads are retracted at which time 5,13 will go negative and break the latch on 3,10. This releases relay R1 and resets (via gate 9,9) JK flip-flop 14,13. Relays R3 and R4 are released. All power to the discs is off.

D24,8 provides a PRESET to the controller logic to reset flip-flops that may have been set by transients when disc power is switched on.

XII. OPERATING NOTES

A. Turn On

1. Have disc packs in place and covers closed.
2. Depress the START pushbutton on Bryant disc units and/or set lever to START on IBM disc units.
3. Press the NORMAL ON pushbutton at the controller.
   a. DC READY should come ON.
   b. AC READY should come ON
   c. After disc cleaning is complete the HEAD EXTENDED indicator should be ON. Cleaning takes about 1 minute.
   d. Unit Available (UA) and READY lights should come on.
4. IGNORE CRC ERROR switch should be set so the indicator is ON.
5. SET WRITE LOCKOUT switch.
6. Depress the REMOTE switch on Bryant units. The white indicator should be ON. On IBM units set the ENABLE/DISABLE switch to ENABLE.
7. On bryant disc units check the READ ONLY pushbutton. This will be green if read only is desired.
8. On Bryant discs check the SELECT CHECK switch. Depress if it is RED. Indicator should go off, if it doesn't, call for help.
9. Check the following indicators on controller panel. If any are lit depress the CLEAR pushbutton - they should go out:
   a. File unsafe
   b. Seek incomplete
   c. Address Error
   d. Illegal Write Address
   e. CRC Error
10. If the indicators in step 10 cannot be cleared and there is an IBM unit on line, stop and restart the IBM discs using the switch on the disc units. After cleaning is complete depress the CLEAR pushbutton. If the above indicators still cannot be cleared there is trouble in the disc or controller.
11. If all the above steps are OK the disc is ready.

B. Run Fail Conditions

1. File Unsafe ON

An unsafe conditon exists in the disc unit. Clear machine, stop and restart IBM units, depress SELECT CHECK on Bryant units, depress CLEAR pushbutton on controller after cleaning operations are complete.

2. Seek Incomplete

a. Indicator comes on if desired cylinder was not located.

b. Clear machine.

c. Depress RTZ pushbutton for each disc on line.

d. Depress CLEAR pushbutton on controller.

3. Address Error

a. A non-existant head or cylinder has been selected.

b. Clear machine.

c. Depress RTZ pushbutton for each disc on line.

d. Depress CLEAR pushbutton on controller.

4. Illegal Write Address

a. Write lockout is on and a cylinder address below 128 was selected for disc module one.

b. Clear machine.

C. Turn Off

1. Depress NORMAL OFF if it is desired to shut down all discs on line.

2. To turn off individual discs on line operate the Start/Stop switch or pushbutton on the disc module desired to be shut down.

3. EMERGENCY OFF should be used ONLY if NORMAL OFF fails. Emergency off shuts down AC and DC power to discs simultaneously and may cause head crashes.

D. Notes on other controller panel indicators

1. Cylinder and head indicators show the current cylinder and head in use.

2. Unit Available (UA) is on when controller is available to accept a command from I/O Control.

3. Ready is on if all discs on line are ready to operate and there are no fail conditions. Ready will not be on during a set disc address operation.

4. Initiate Read, Initiate Write, Set Disc Address (SDA). These indicators are on during a read, write or set disc address command.

5. Select Module indicates which disc has been selected.

ORDER		TRUNK	O.T.	E.A.	E.A.	C2
Set Disc Address		(A)	ø8	(A_1)	(øøøøø)	(ø42ø3)
Set Disc Address		(A)	ø8	(A_1)	(øøøøø)	(ø42øS)
Set Disc Address		(A)	ø8	(A_1)	(øøøøø)	(ø62ø3)
Set Disc Address		(A)	ø8	(A_1)	(øøøøø)	(ø62øS)
Set Disc Address		(B)	ø8	(A_1)	(øøøøø)	(ø42ø5)
Set Disc Address		(B)	ø8	(A_1)	(øøøøø)	(ø42øJ)
Set Disc Address		(B)	ø8	(A_1)	(øøøøø)	(ø62ø5)
Set Disc Address		(B)	ø8	(A_1)	(øøøøø)	(ø62øJ)
Write	8x72	(A)	ø8	(A_2)	(B)	(ø61øK)
Write	8x64	(A)	ø8	(A_2)	(B)	(ø61ø2)
Write	8x72	(B)	ø8	(A_2)	(B)	(ø61øN)
Write	8x64	(B)	ø8	(A_2)	(B)	(ø61ø4)
Read	8x72	(A)	ø8	(A_2)	(B)	(ø6øøS)
Read	8x64	(A)	ø8	(A_2)	(B)	(ø6øø3)
Read	8x72	(B)	ø8	(A_2)	(B)	(ø6øøJ)
Read	8x64	(B)	ø8	(A_2)	(B)	(ø6øø5)

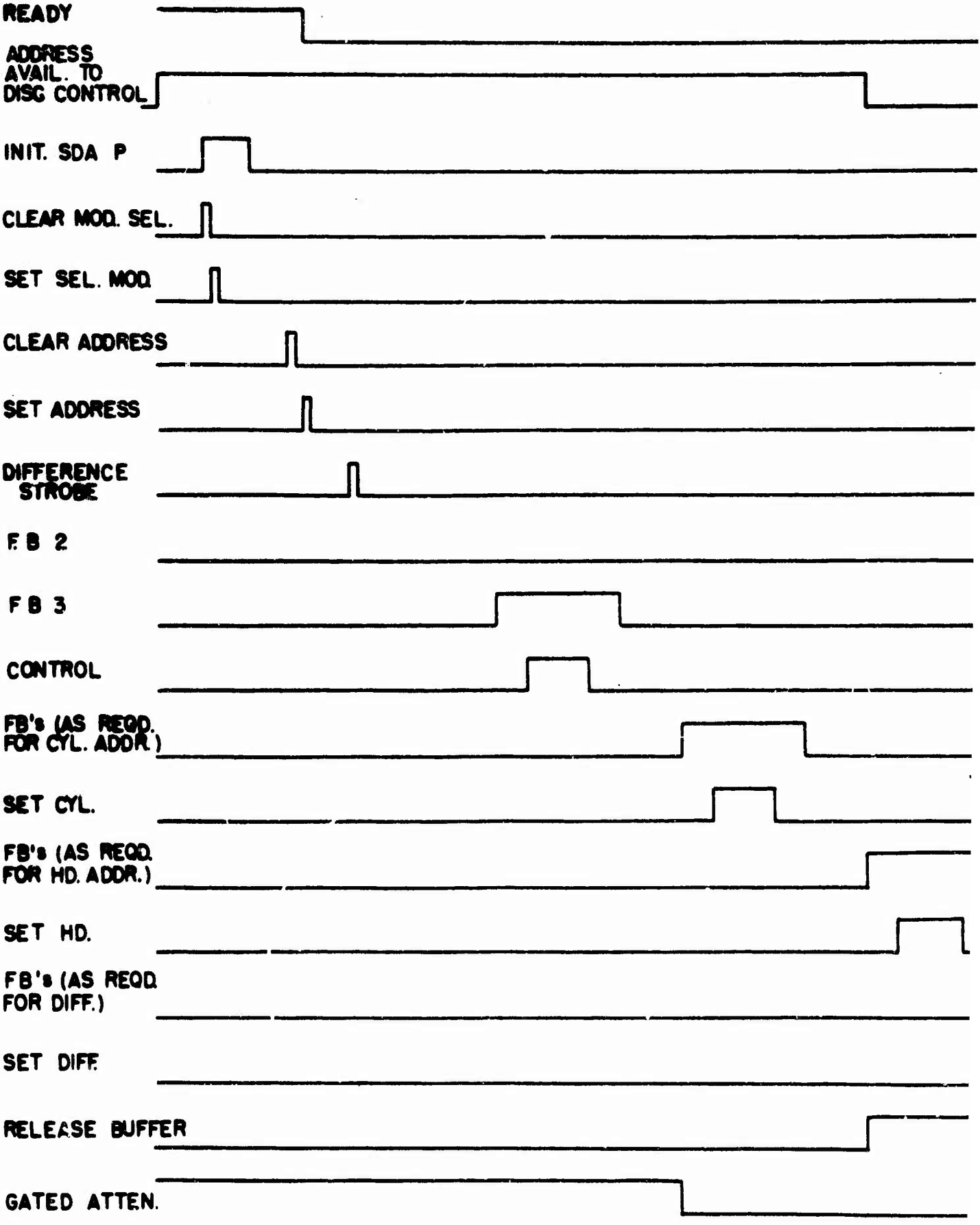
A_1 -- Disc unit, cylinder, head as desired
bits 55-56 select units øø, ø1, ø2, ø3
bits 45-52 select cylinder ø to øNK
bits 41-44 select head ø to 9

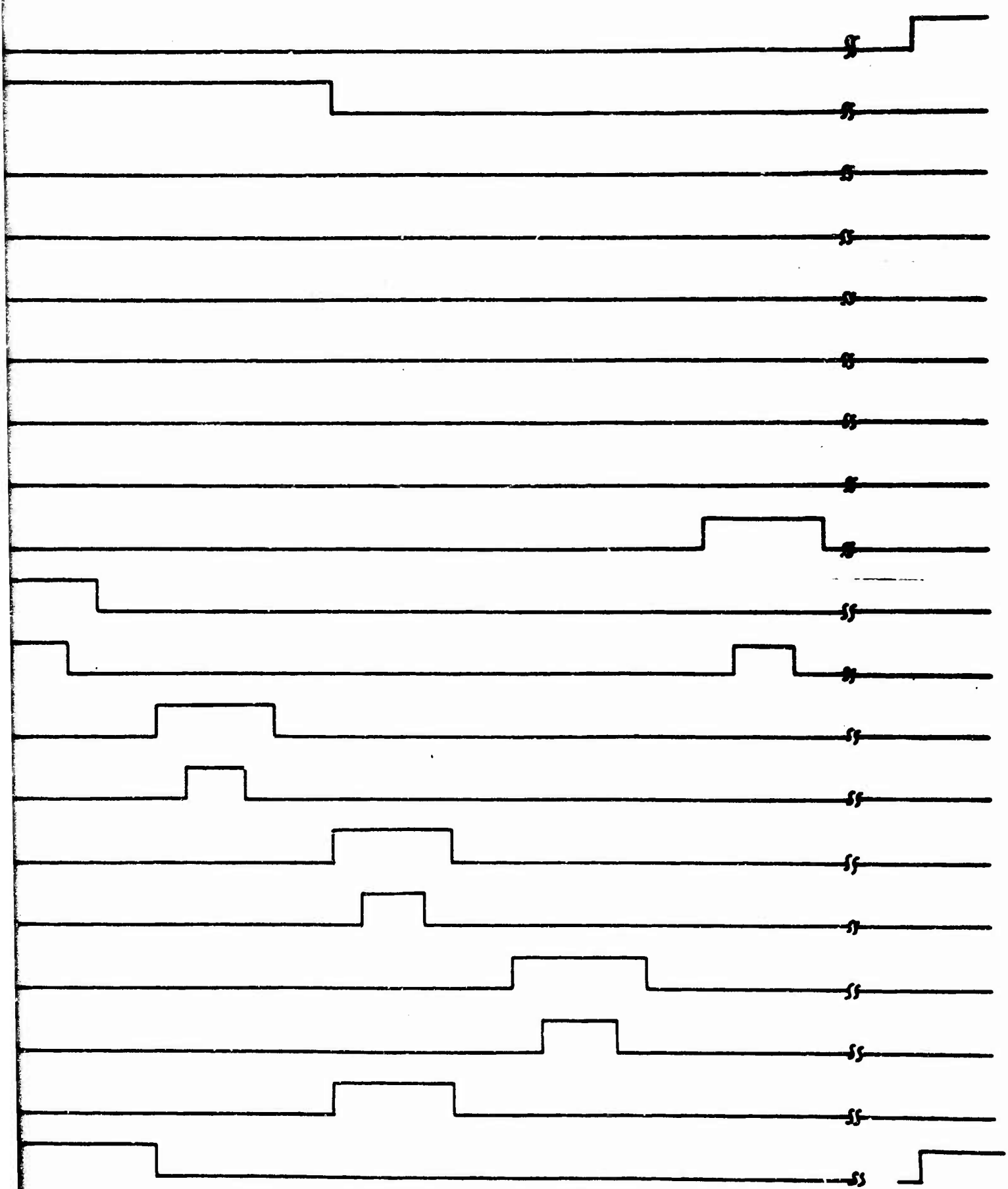
A_2 -- Select location at which data transfer is to start from

B -- Select number of words to be transferred

TABLE I

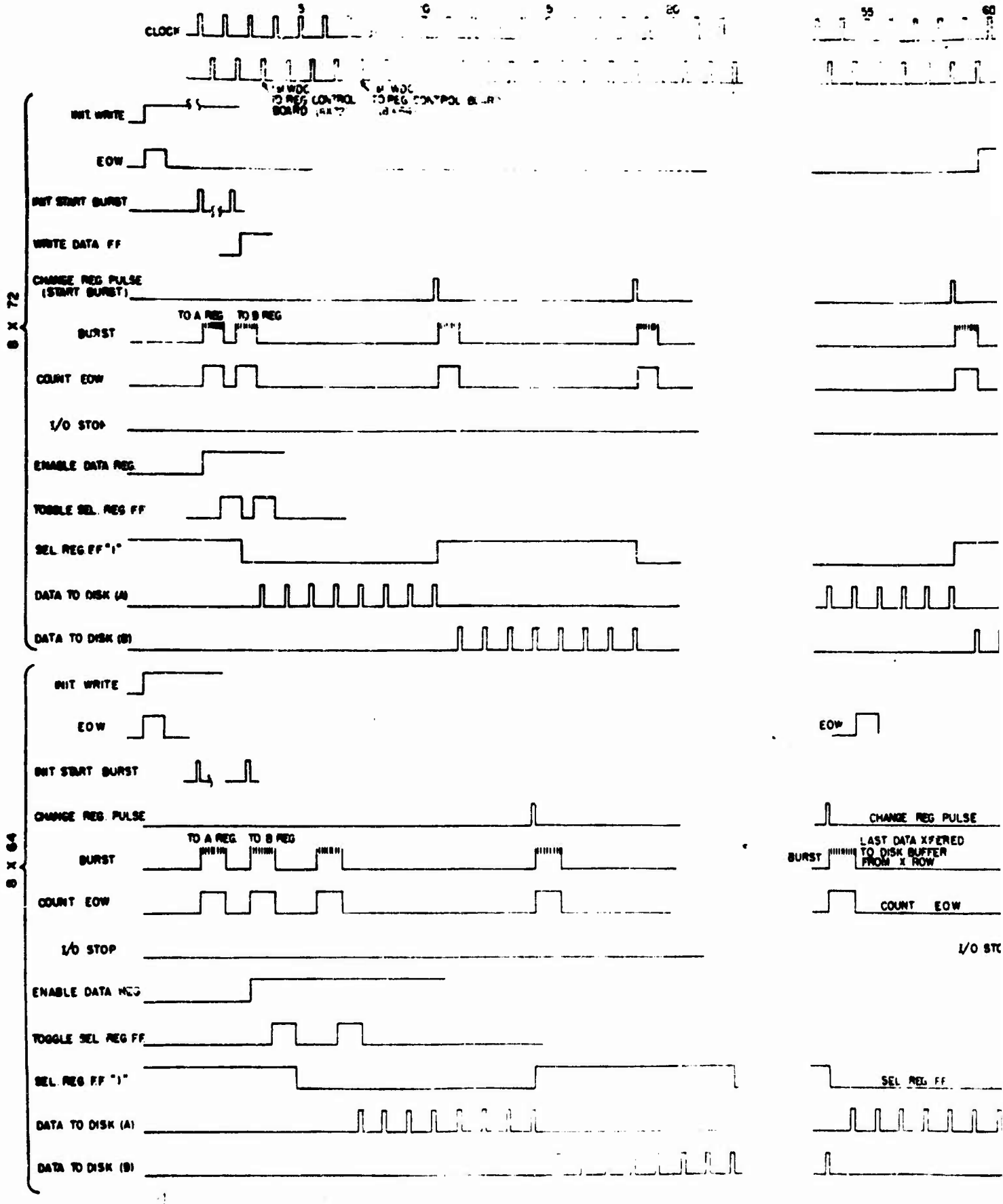
DISC ORDERS

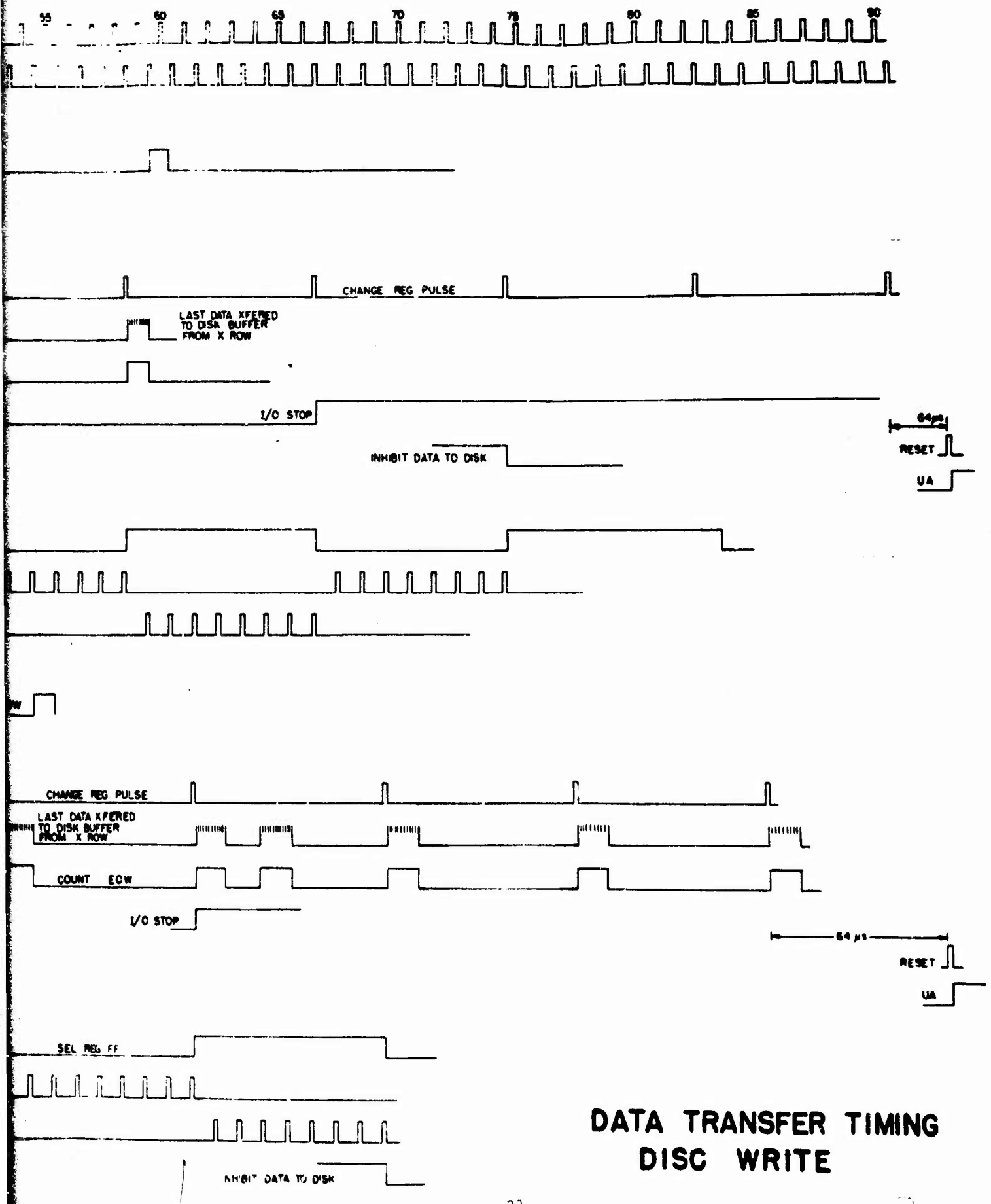

READY
ADDRESS AVAIL. TO DISC CONTROL
INIT. SDA P
CLEAR MOD. SEL.
SET SEL. MOD
CLEAR ADDRESS
SET ADDRESS
DIFFERENCE STROBE
F B 2
F B 3
CONTROL
FB's (AS REQD. FOR CYL. ADDR.)
SET CYL.
FB's (AS REQD. FOR HD. ADDR.)
SET HD.
FB's (AS REQD. FOR DIFF.)
SET DIFF.
RELEASE BUFFER
GATED ATTEN.



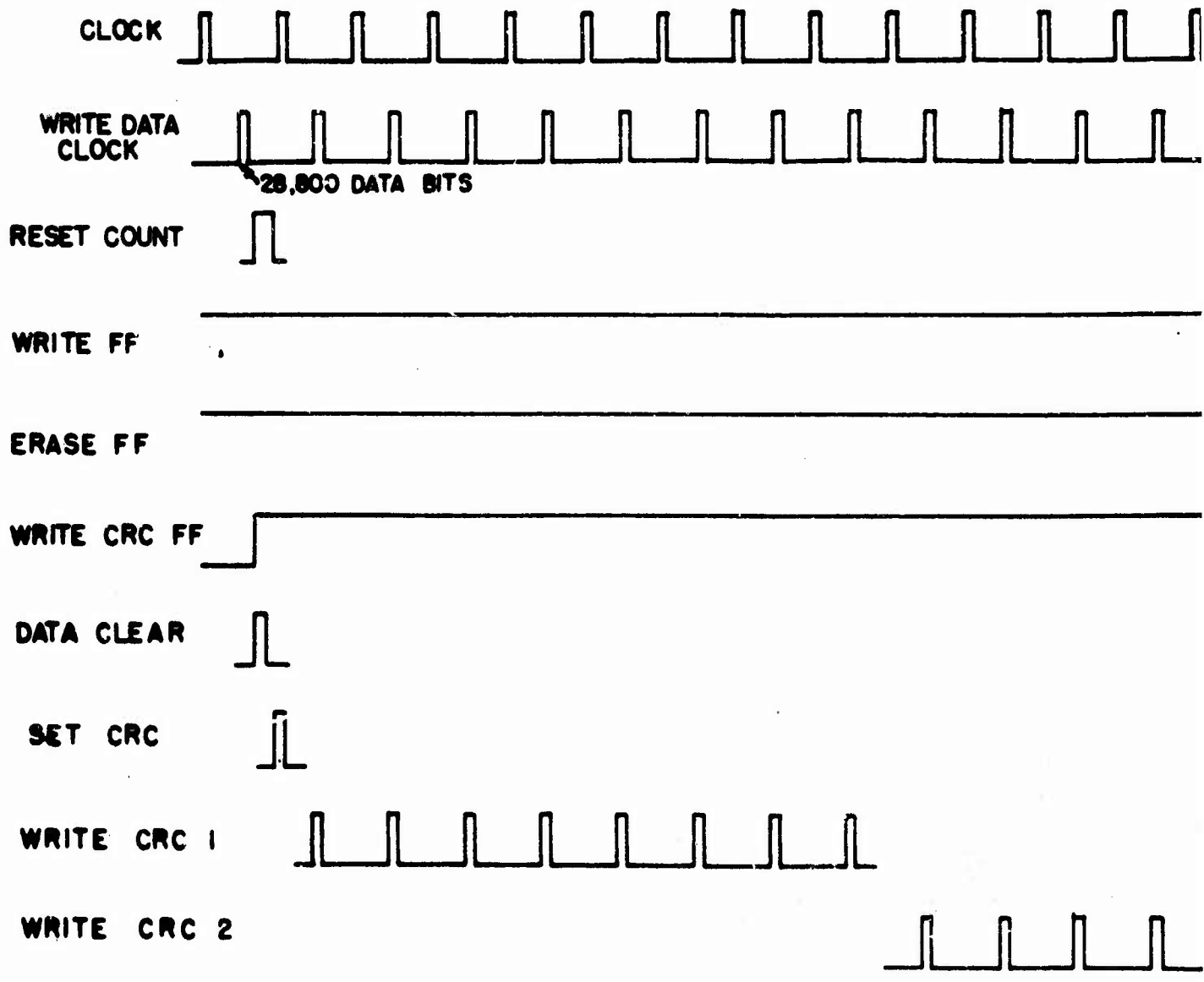
SDA TIMING

B


CLOCK
INIT WRITE
EOW
INIT START BURST
WRITE DATA FF
CHANGE REG PULSE (START BURST)
TO A REG
TO B REG
BURST
COUNT EOW
I/O STOP
ENABLE DATA REG
TOGGLE SEL. REG FF
SEL REG FF "1"
DATA TO DISK (A)
DATA TO DISK (B)
8 X 72
INIT WRITE
EOW
INIT START BURST
CHANGE REG. PULSE
TO A REG
TO B REG
BURST
COUNT EOW
I/O STOP
ENABLE DATA REG
TOGGLE SEL REG FF
SEL REG FF "1"
DATA TO DISK (A)
DATA TO DISK (B)
8 X 64
EOW
CHANGE REG PULSE
LAST DATA XFERED TO DISK BUFFER FROM X ROW
COUNT EOW
SEL REG FF

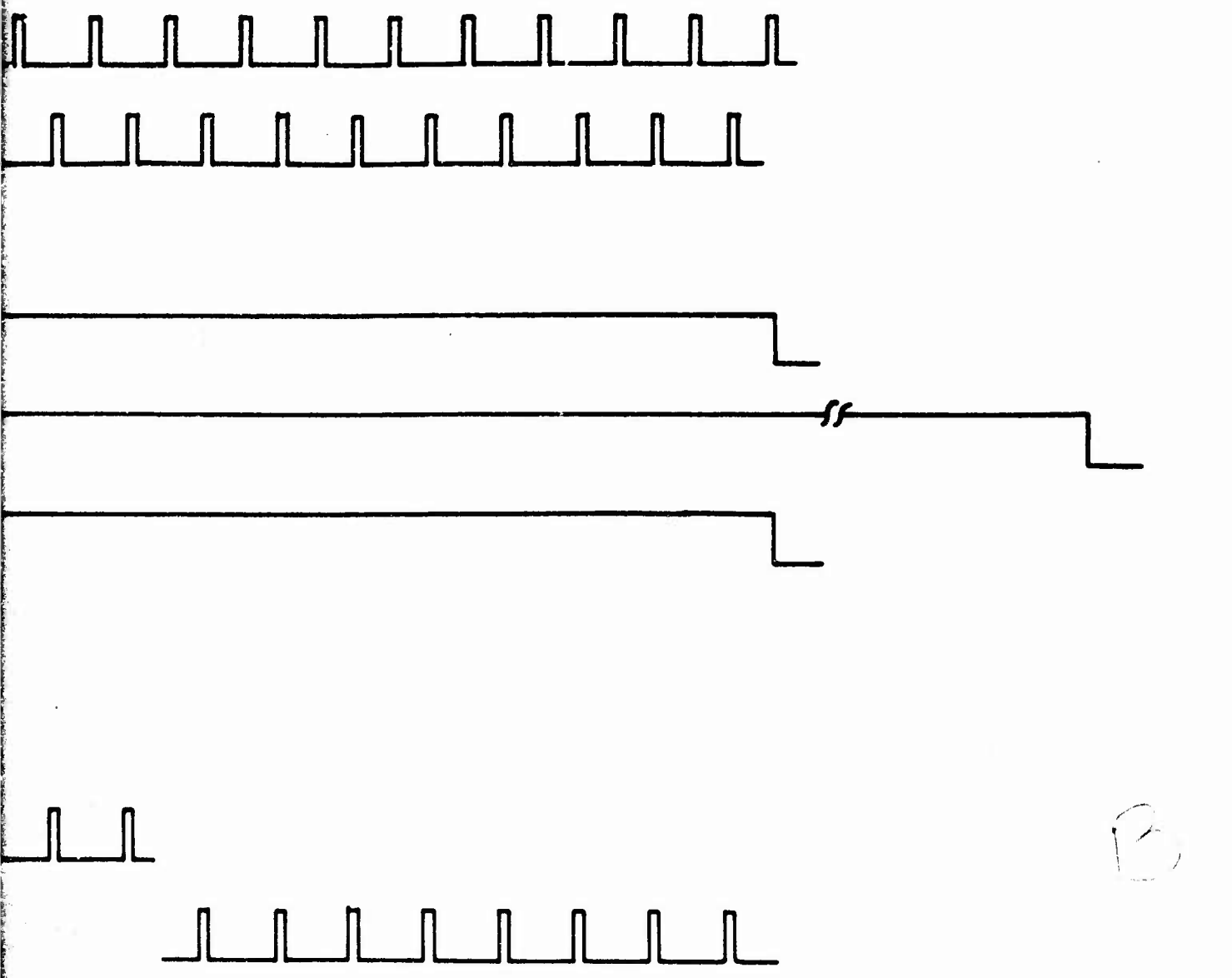


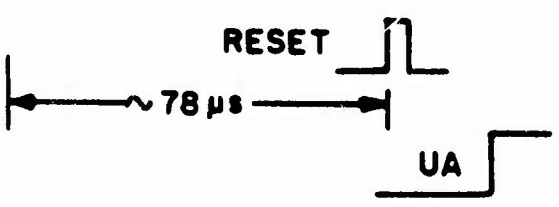
DATA TRANSFER TIMING
DISC WRITE


CLOCK
WRITE DATA CLOCK
28,800 DATA BITS
RESET COUNT
WRITE FF
ERASE FF
WRITE CRC FF
DATA CLEAR
SET CRC
WRITE CRC 1
WRITE CRC 2

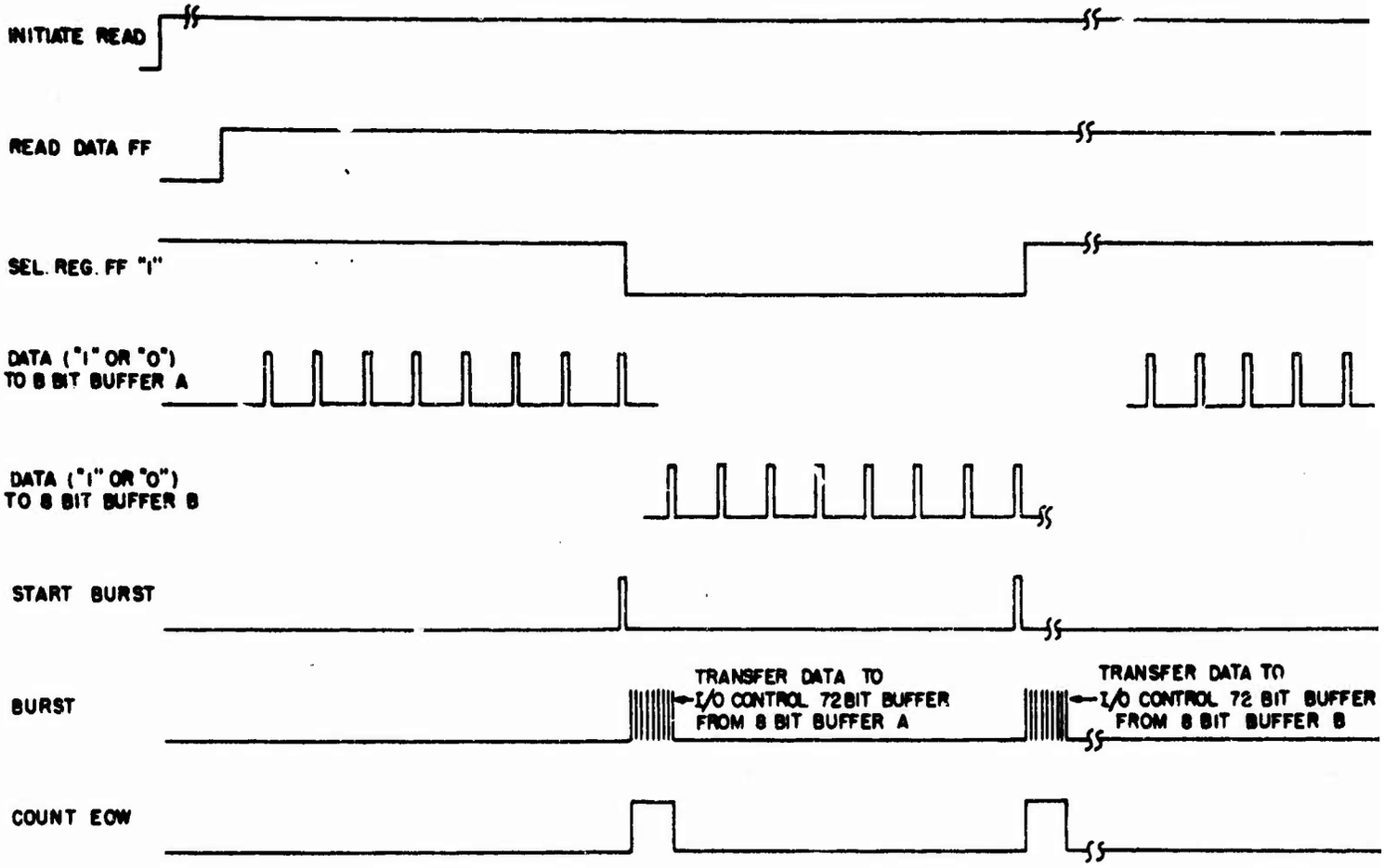
A

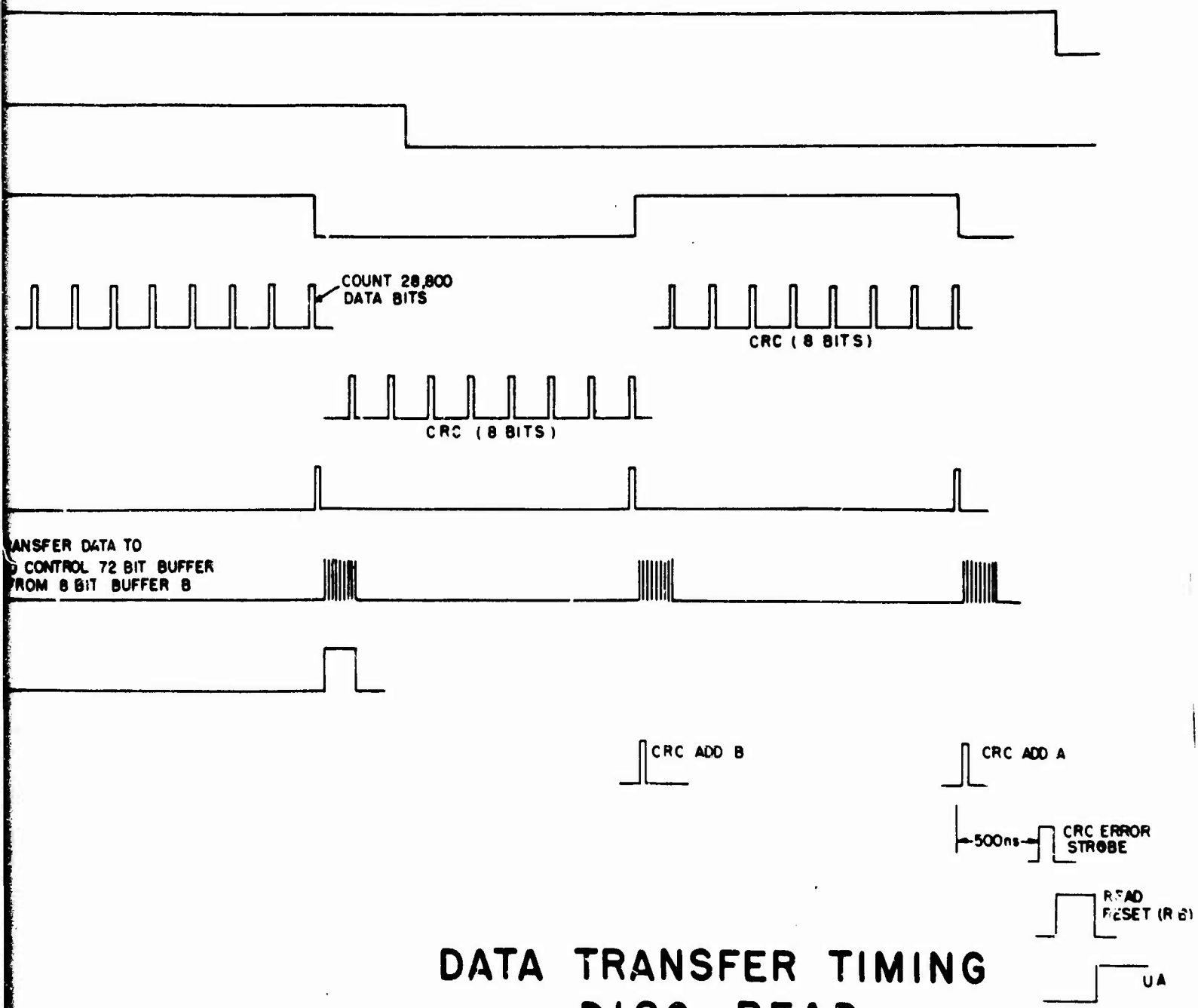
WR



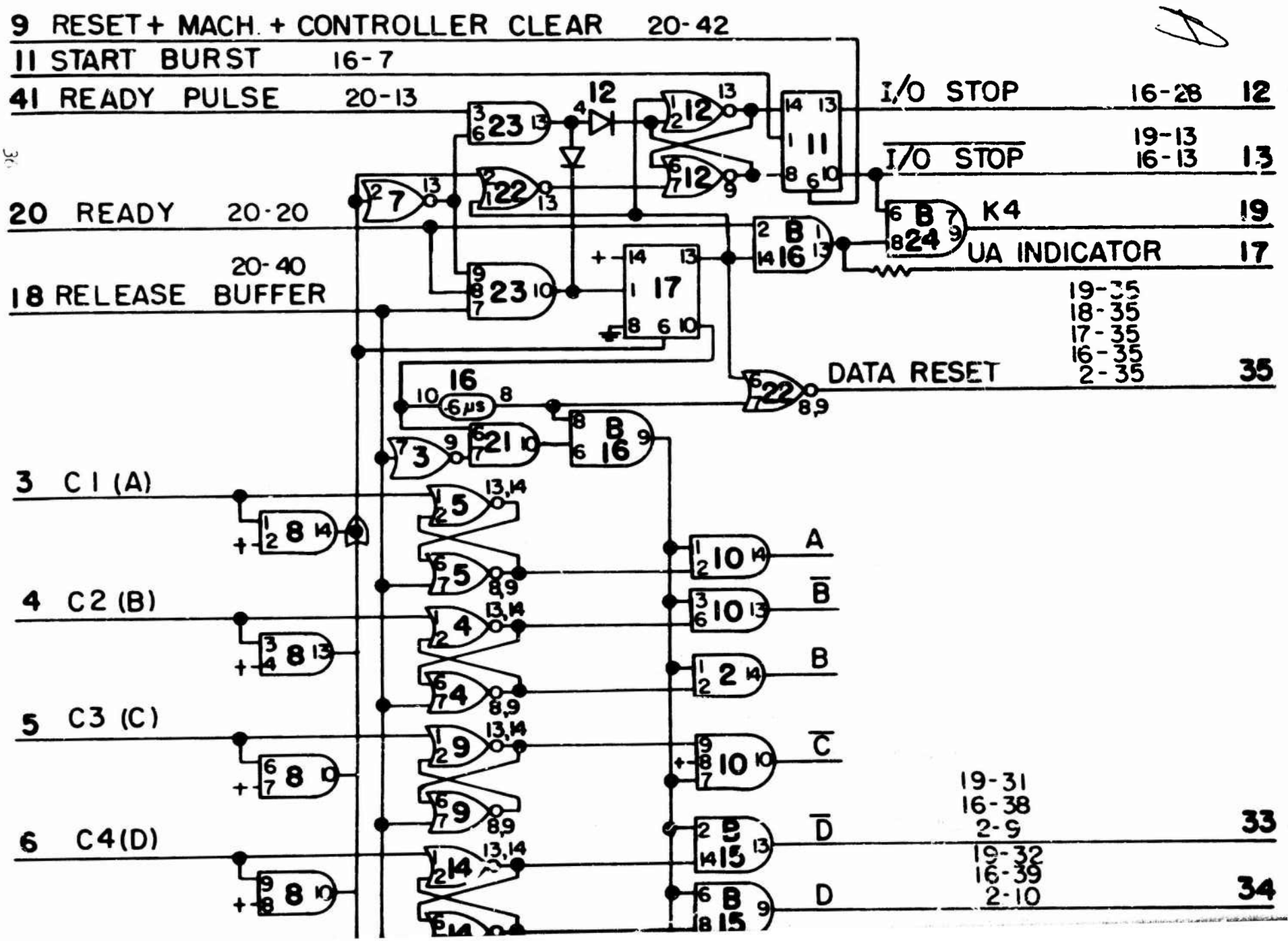


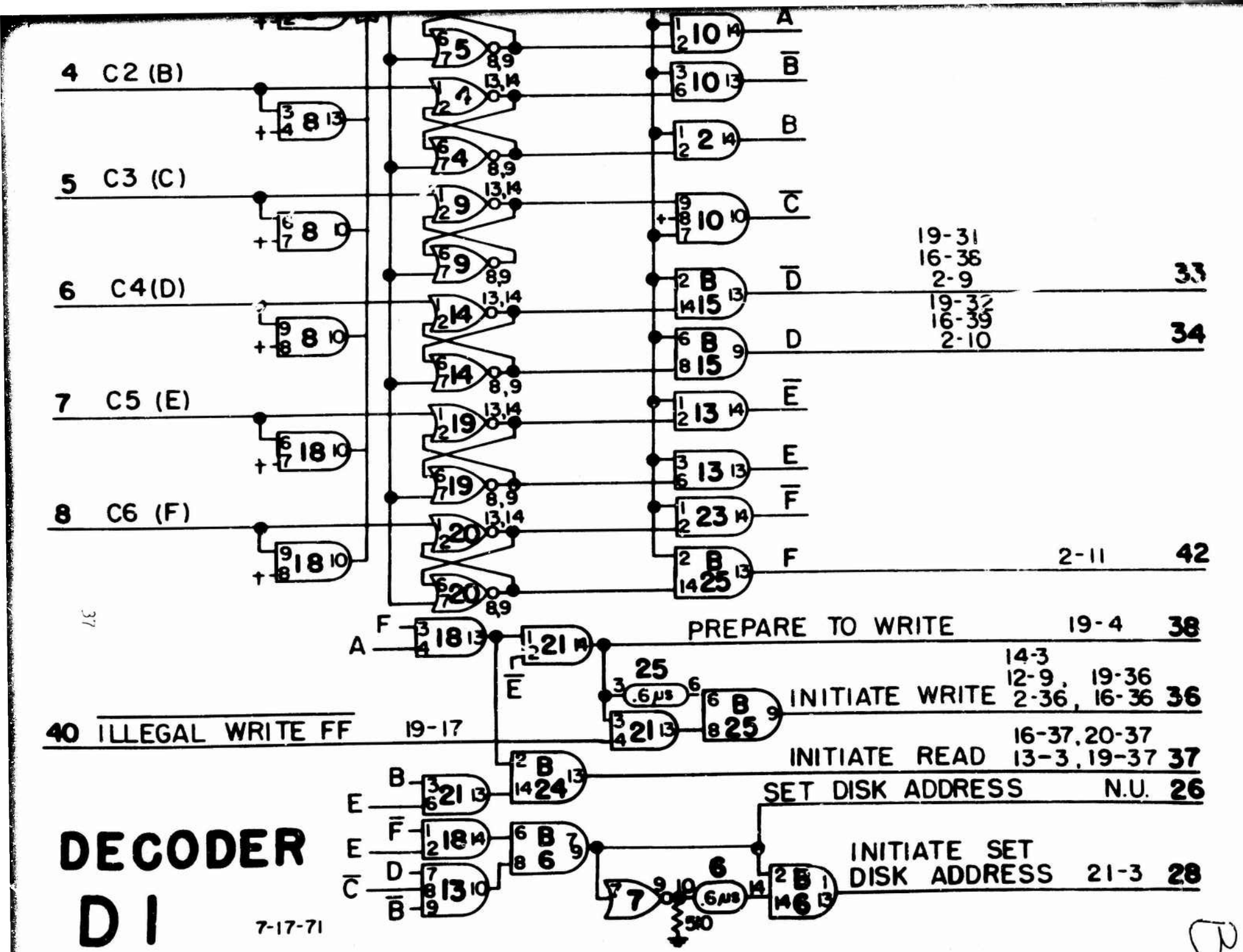
WRITE CRC TIMING

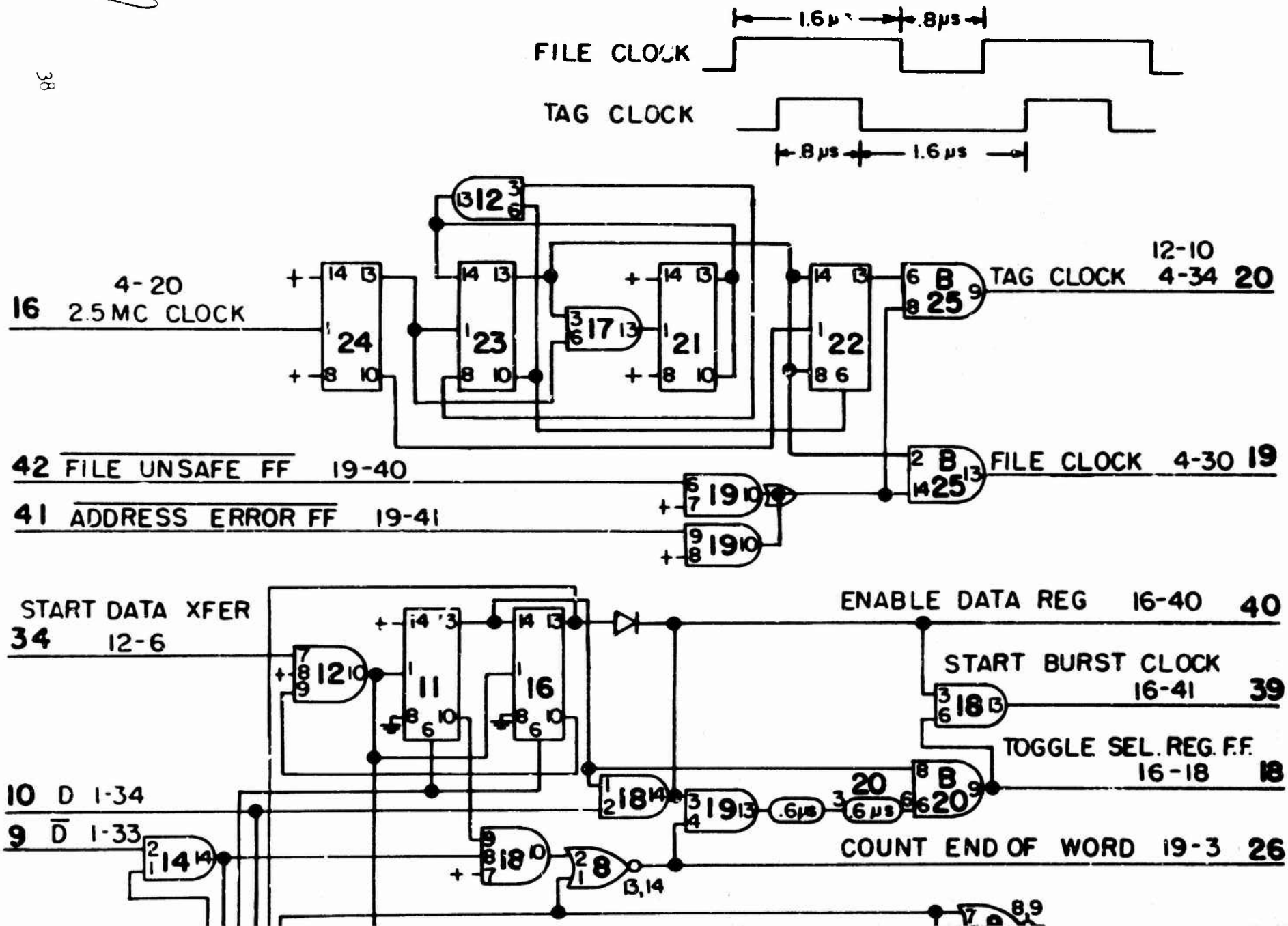

INITIATE READ
READ DATA FF
SEL. REG. FF "1"
DATA ("1" OR "0") TO 8 BIT BUFFER A
DATA ("1" OR "0") TO 8 BIT BUFFER B
START BURST
BURST
TRANSFER DATA TO I/O CONTROL 72 BIT BUFFER FROM 8 BIT BUFFER A
TRANSFER DATA TO I/O CONTROL 72 BIT BUFFER FROM 8 BIT BUFFER B
COUNT EOW

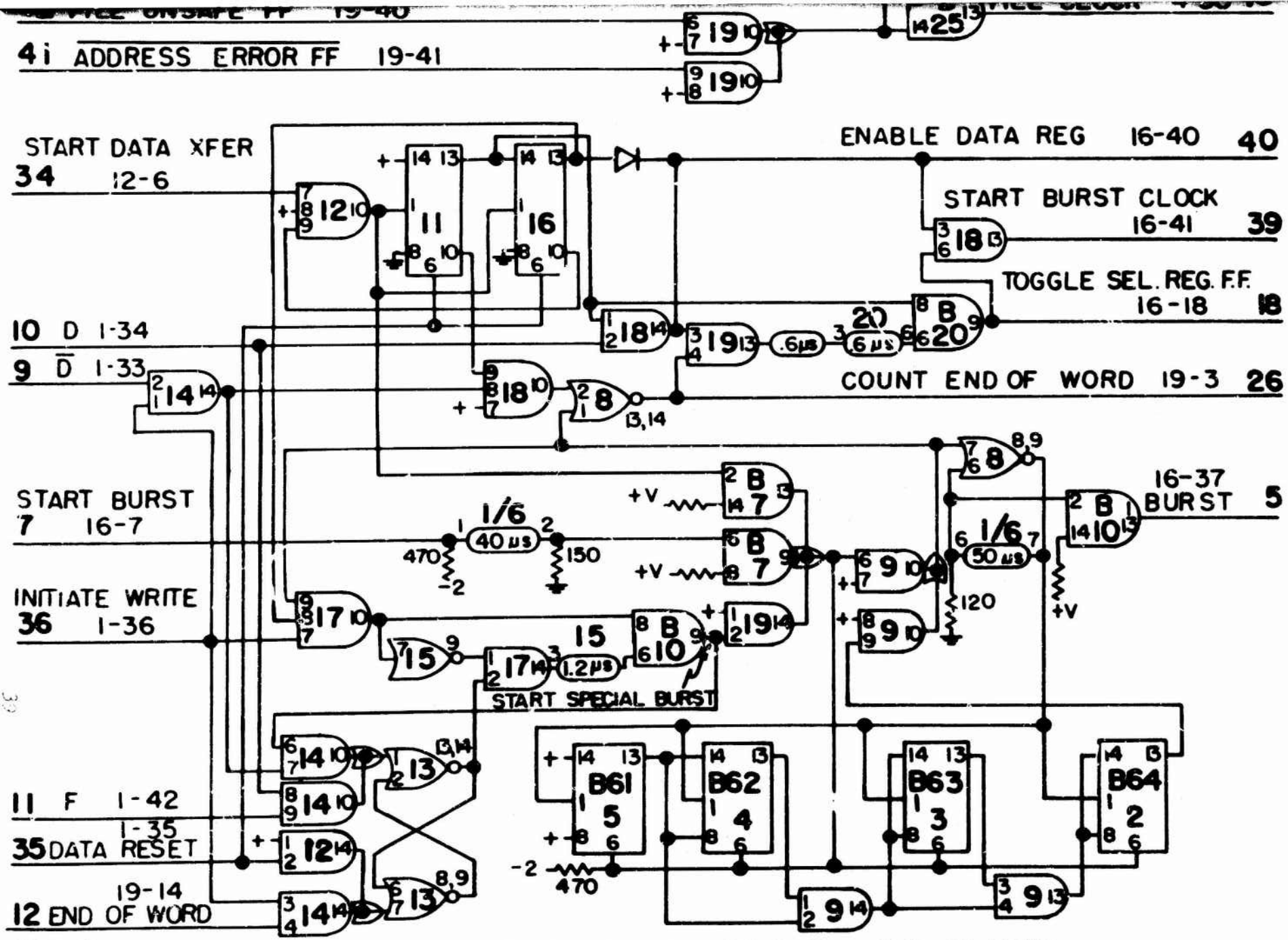


DATA TRANSFER TIMING
DISC READ


9 RESET + MACH. + CONTROLLER CLEAR 20-42
11 START BURST 16-7
41 READY PULSE 20-13
20 READY 20-20
18 RELEASE 20-40 BUFFER
3 C1 (A)
4 C2 (B)
5 C3 (C)
6 C4 (D)
I/O STOP 16-28 12
I/O STOP 19-13 16-13 13
K4 19
UA INDICATOR 17
DATA RESET 19-35 18-35 17-35 16-35 2-35 35
A
B
C
D
19-31 16-38 2-9 33
19-32 16-39 2-10 34


4 C2 (B)
5 C3 (C)
6 C4(D)
7 C5 (E)
8 C6 (F)
A
B̄
B
C̄
D̄
D
Ē
E
F̄
F
19-31
16-36
2-9
33
19-32
16-39
2-10
34
2-11
42
PREPARE TO WRITE
19-4
38
14-3
12-9, 19-36
2-36, 16-36
INITIATE WRITE
36
40 ILLEGAL WRITE FF
19-17
16-37, 20-37
13-3, 19-37
INITIATE READ
37
SET DISK ADDRESS
N.U.
26
INITIATE SET
DISK ADDRESS
21-3
28
.6μs
510
DECODER
D1
7-17-71


1.6 μs
.8μs
FILE CLOCK
TAG CLOCK
.8 μs
1.6 μs
4-20
16 2.5MC CLOCK
12-10
TAG CLOCK 4-34 20
42 FILE UNSAFE FF 19-40
41 ADDRESS ERROR FF 19-41
FILE CLOCK 4-30 19
START DATA XFER
34 12-6
ENABLE DATA REG 16-40 40
START BURST CLOCK
16-41 39
TOGGLE SEL. REG. F.F.
16-18 18
10 D 1-34
9 D̄ 1-33
.6μs
.6 μs
COUNT END OF WORD 19-3 26
13,14
8,9



D2 BURST GEN. FILE & TAG CLOCK

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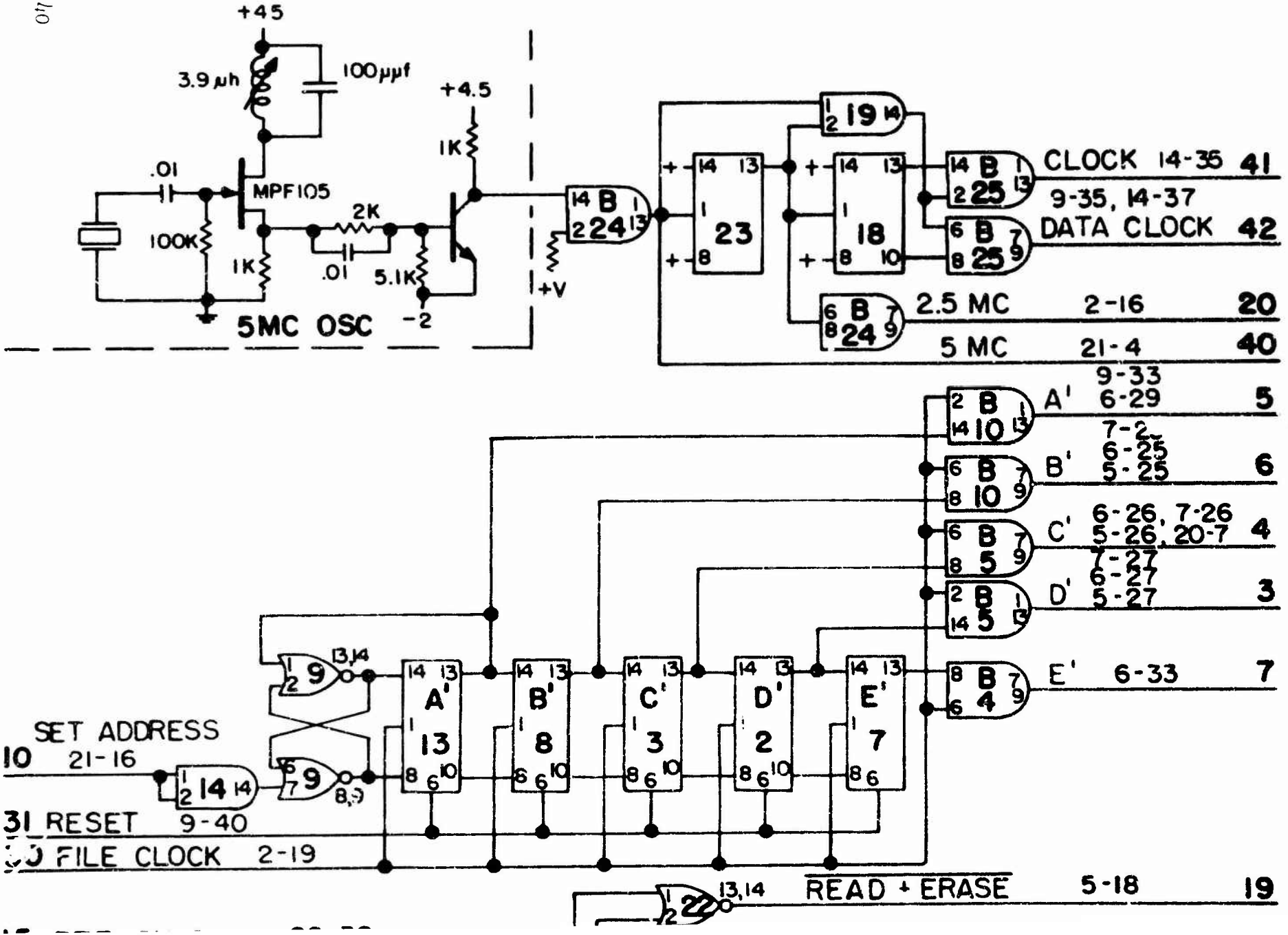
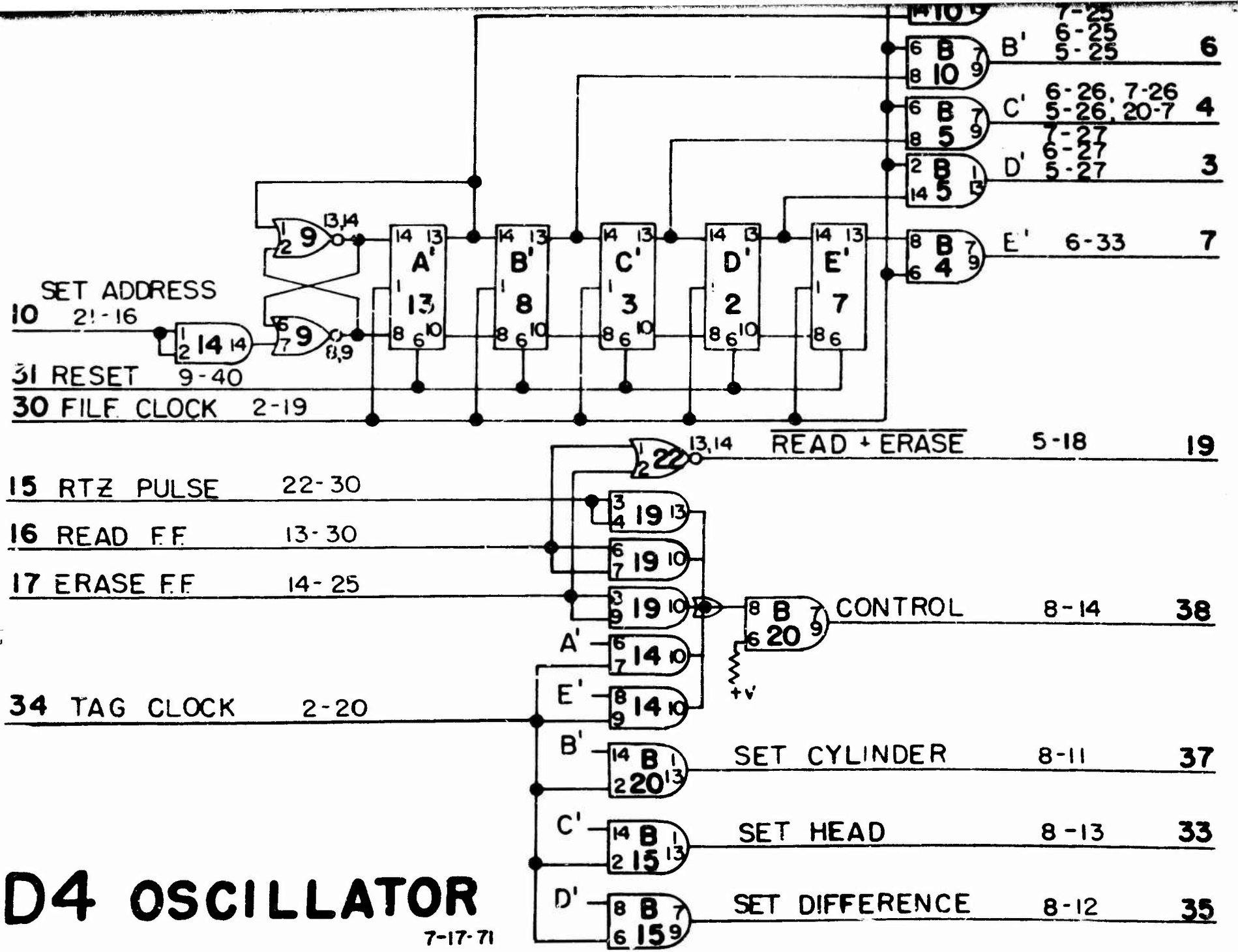

+45
3.9 µh
100µµf
+4.5
1K
.01
MPF105
2K
100K
1K
.01
5.1K
-2
+V
5MC OSC
CLOCK 14-35 41
9-35, 14-37
DATA CLOCK 42
2.5 MC 2-16 20
5 MC 21-4 40
A' 9-33 6-29 5
B' 7-2, 6-25 5-25 6
C' 6-26, 7-26 5-26, 20-7 4
D' 7-27 6-27 5-27 3
E' 6-33 7
SET ADDRESS
10 21-16
31 RESET 9-40
FILE CLOCK 2-19
READ + ERASE 5-18 19



D4 OSCILLATOR

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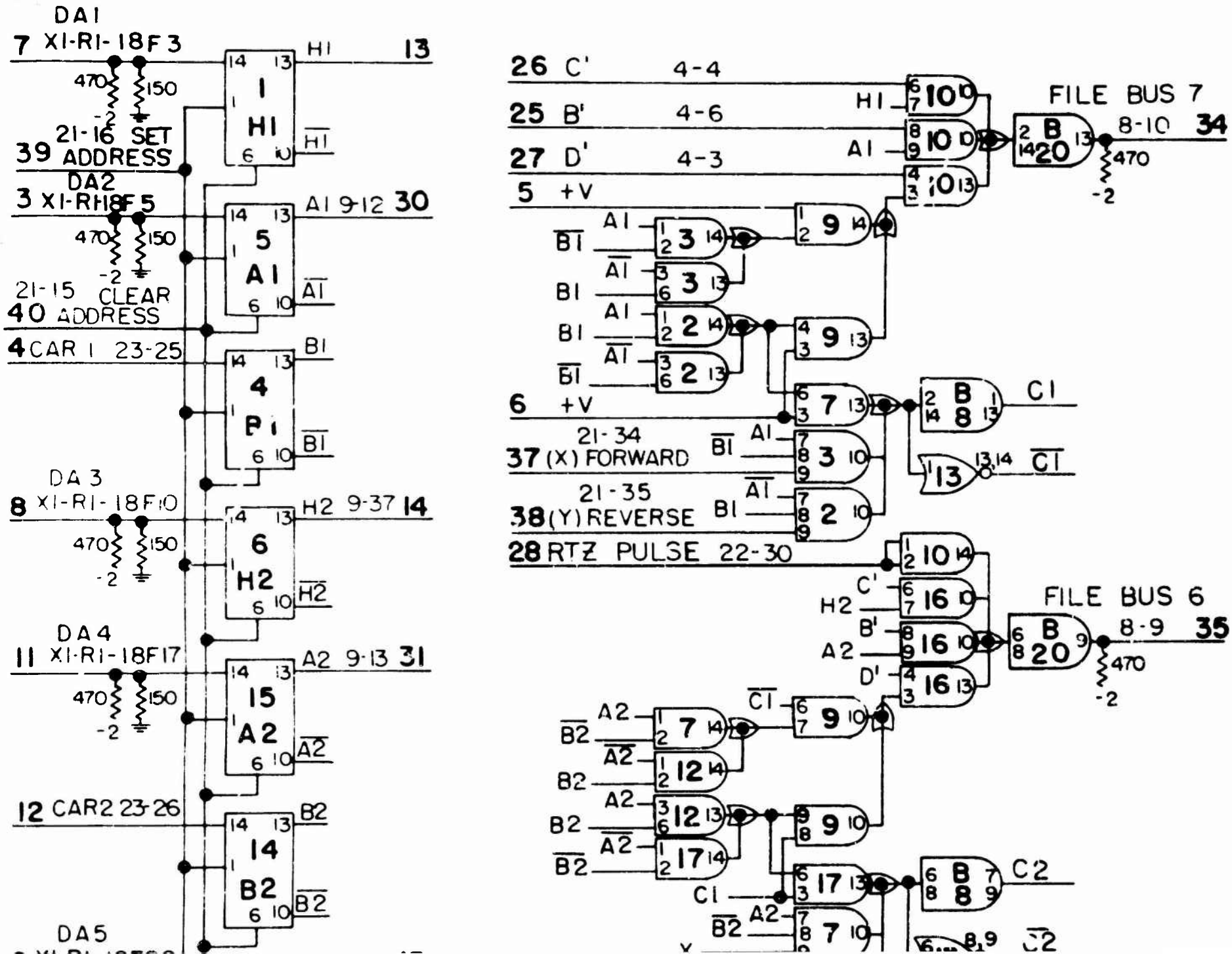
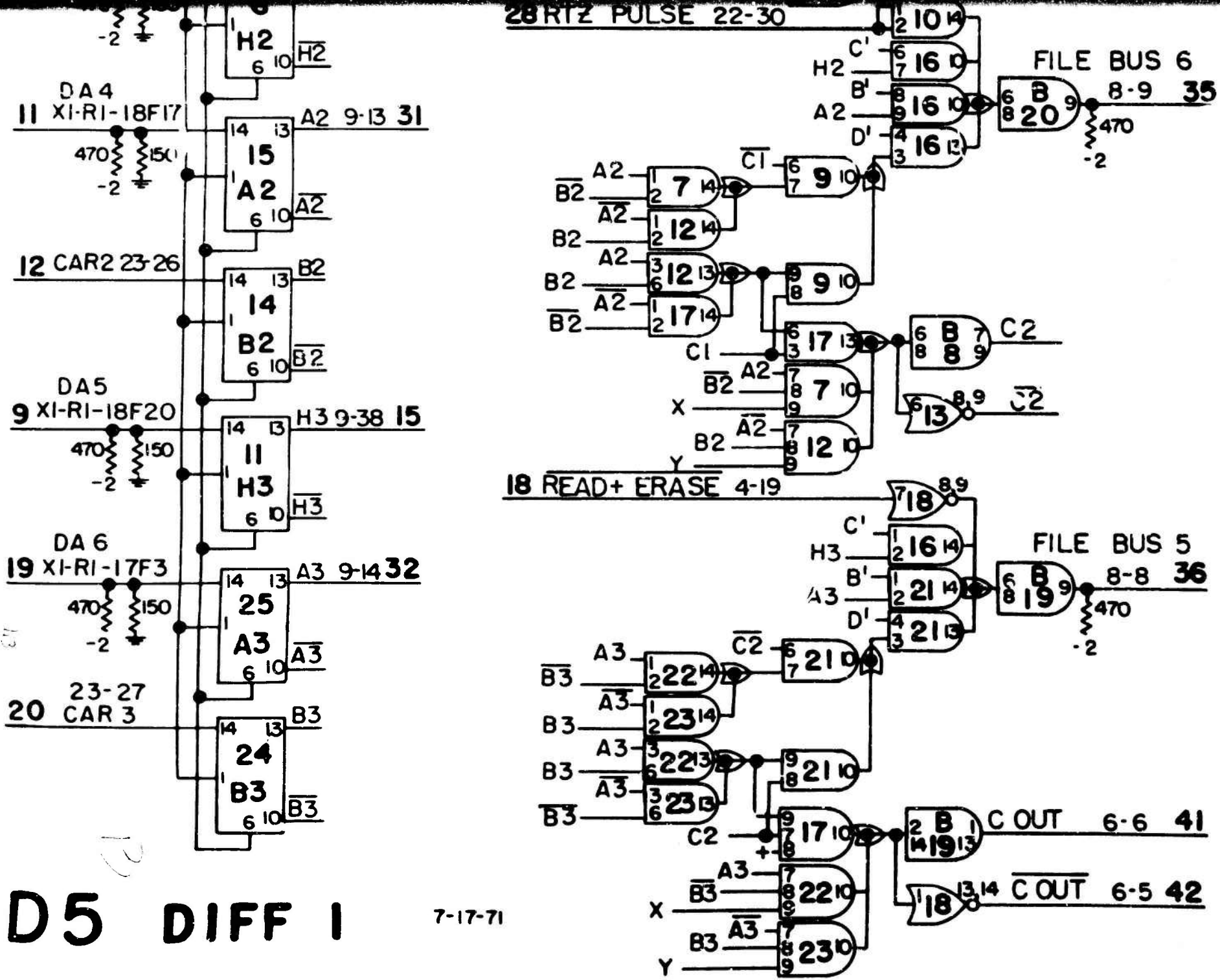

DA1
7 X1-R1-18F3
470
150
-2
21-16 SET
39 ADDRESS
DA2
3 X1-R1-18F5
21-15 CLEAR
40 ADDRESS
4 CAR 1 23-25
DA 3
8 X1-R1-18F10
DA4
11 X1-R1-18F17
12 CAR2 23-26
DA5
H1
13
A1 9-12 30
B1
H2 9-37 14
A2 9-13 31
B2
1
H1
5
A1
4
B1
6
H2
15
A2
14
B2
26 C' 4-4
25 B' 4-6
27 D' 4-3
5 +V
6 +V
21-34
37 (X) FORWARD
21-35
38 (Y) REVERSE
28 RTZ PULSE 22-30
FILE BUS 7
8-10 34
FILE BUS 6
8-9 35
C1
C2


DA 4
11 XI-RI-18F17
12 CAR2 23-26
DA 5
9 XI-RI-18F20
DA 6
19 XI-RI-17F3
23-27
20 CAR 3
28 RTZ PULSE 22-30
18 READ+ ERASE 4-19
FILE BUS 6
FILE BUS 5
C OUT 6-6 41
C OUT 6-5 42
D5 DIFF 1
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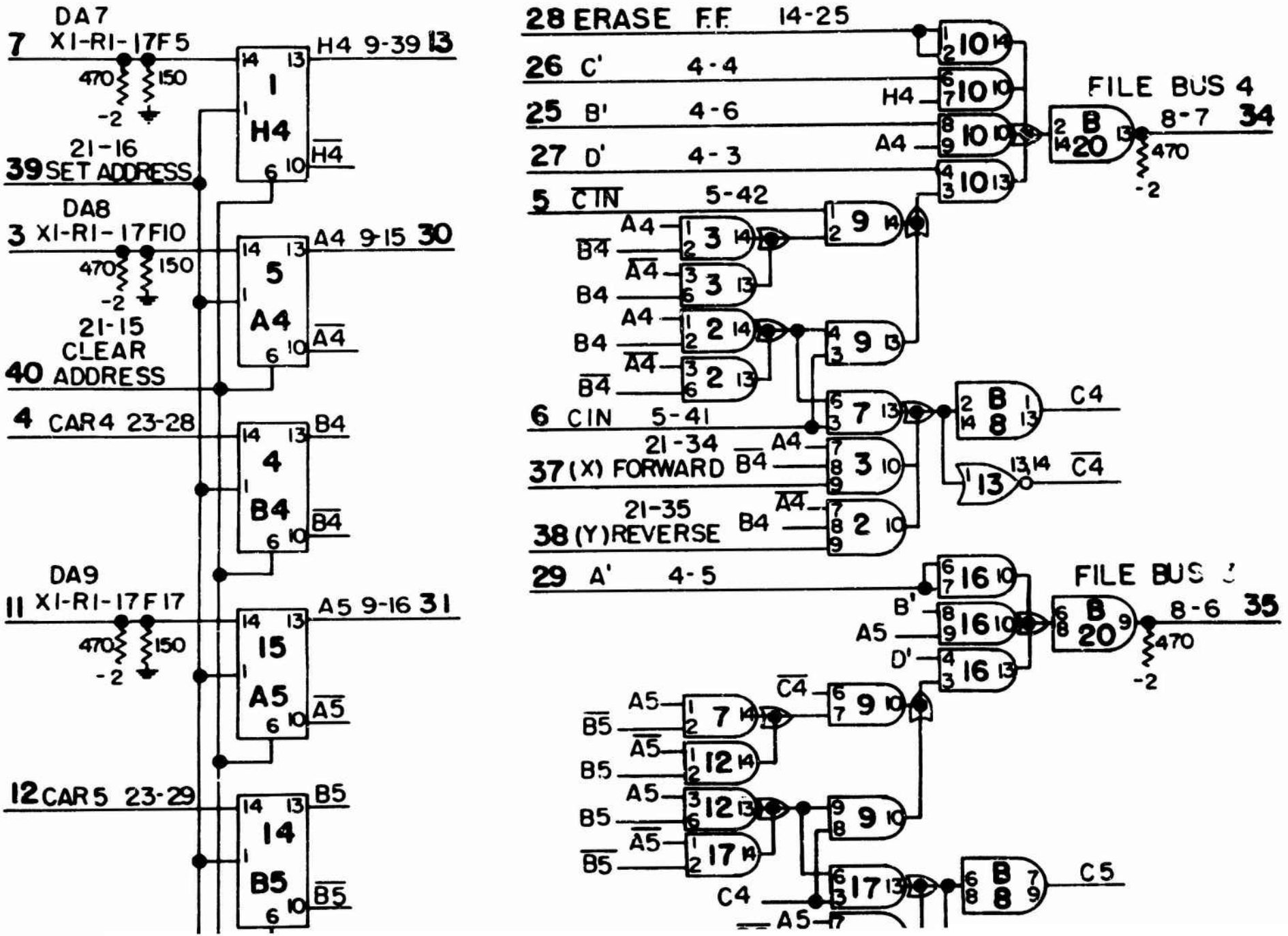
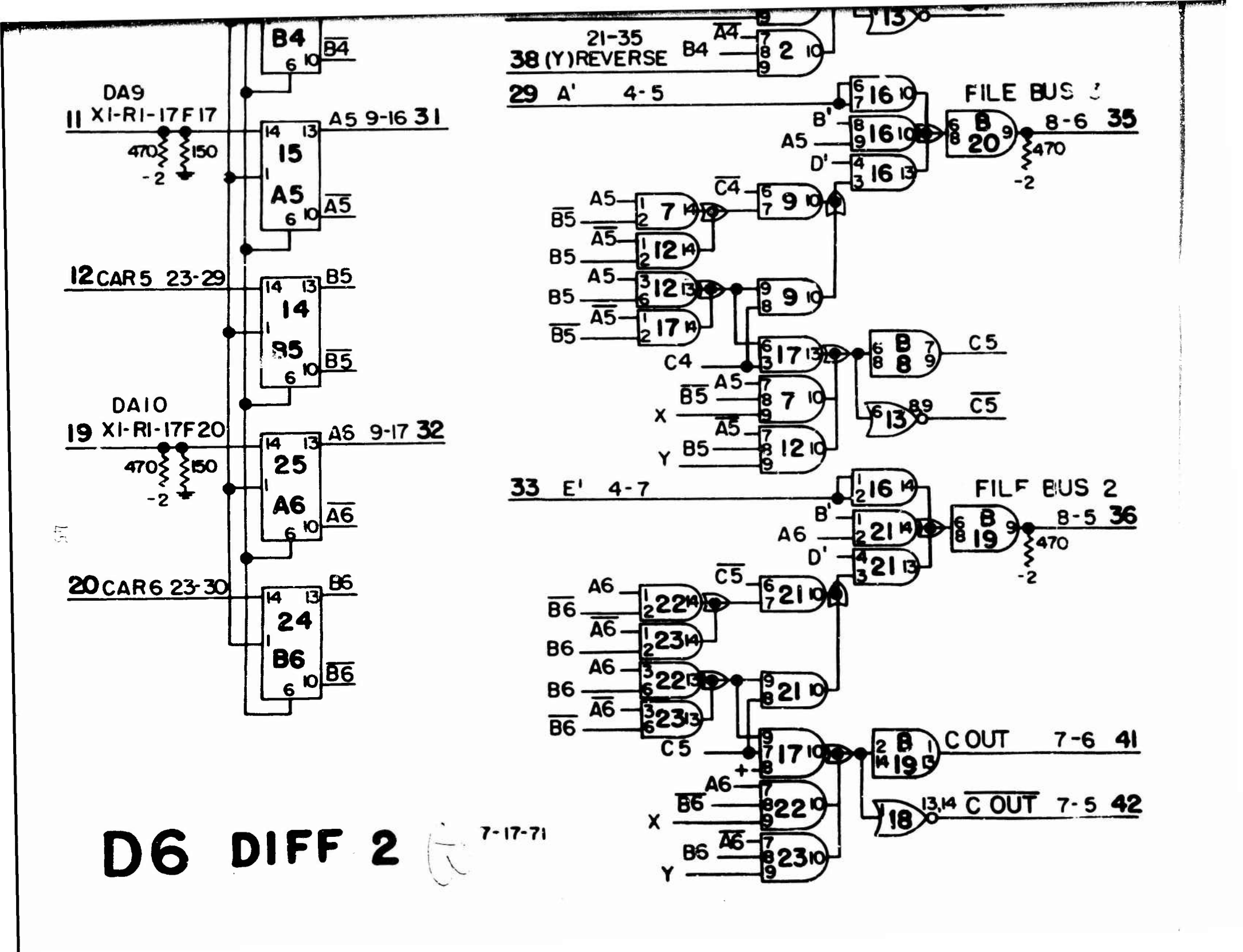
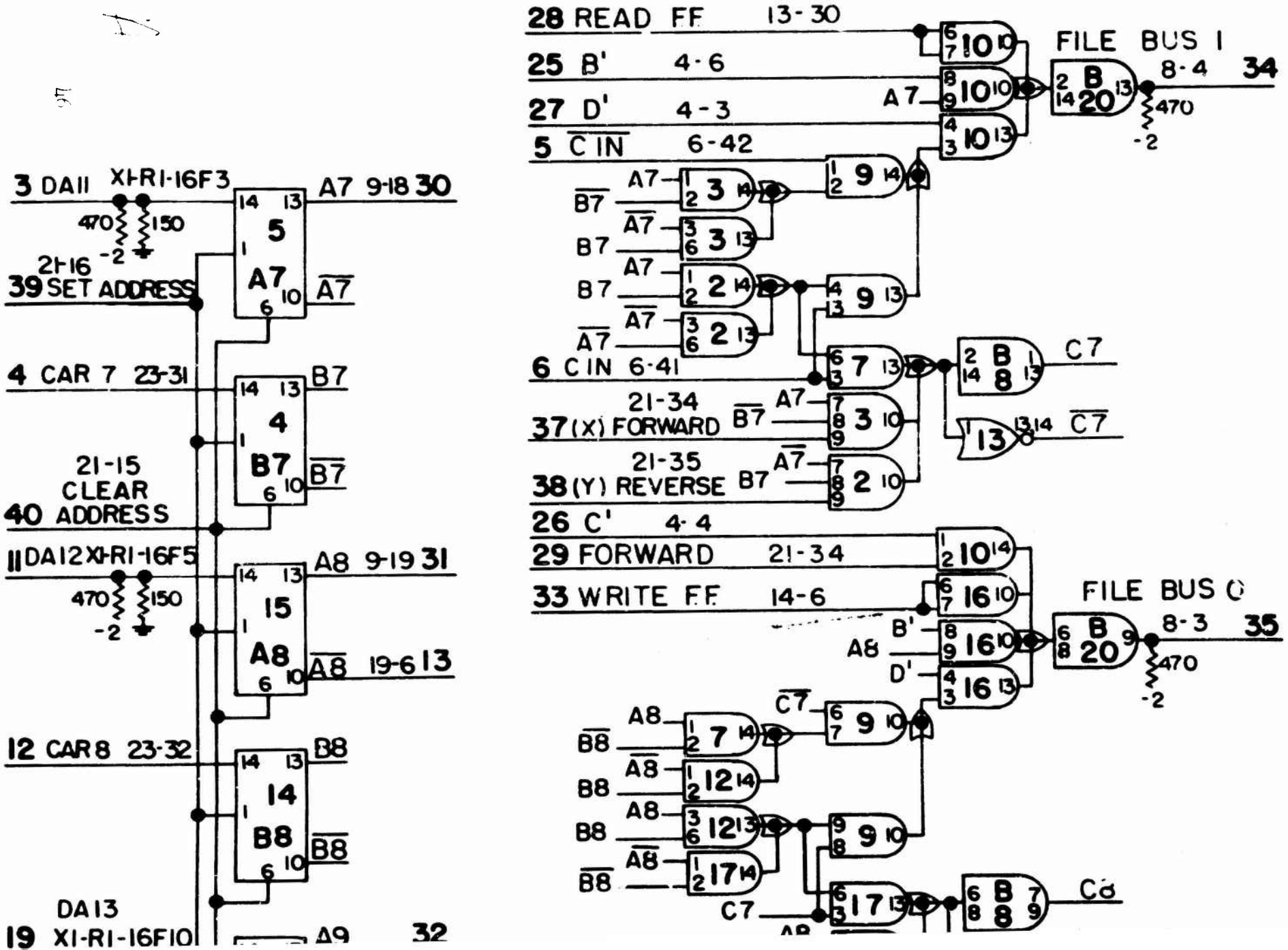
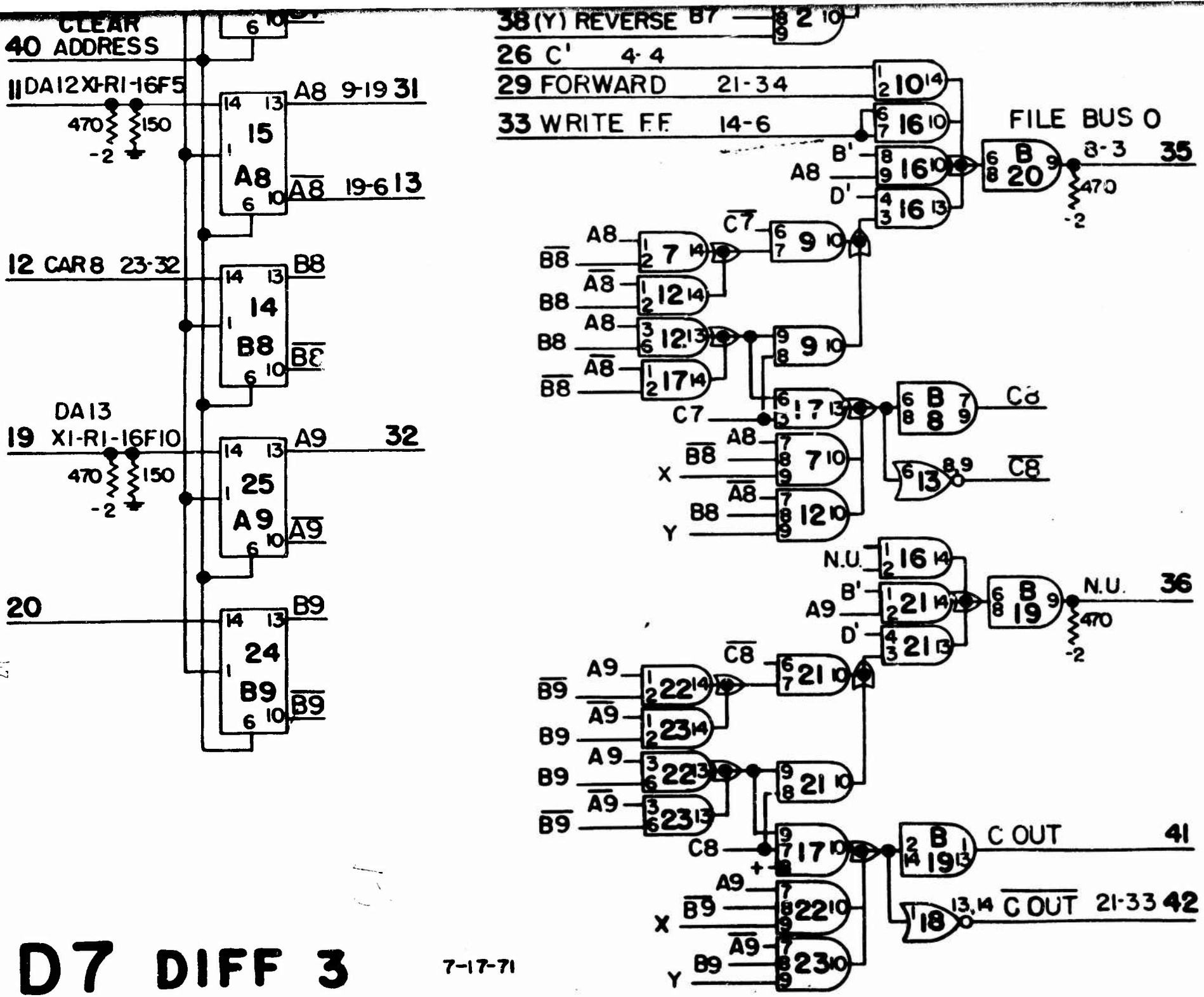

DA7
7 X1-RI-17F5
470
150
-2
H4 9-39 13
21-16
39 SET ADDRESS
DA8
3 X1-RI-17F10
A4 9-15 30
21-15
CLEAR
40 ADDRESS
4 CAR4 23-28
B4
DA9
11 X1-RI-17F17
A5 9-16 31
12 CAR5 23-29
B5
28 ERASE F.F. 14-25
26 C' 4-4
25 B' 4-6
27 D' 4-3
5 CTN 5-42
6 CIN 5-41
21-34
37 (X) FORWARD
21-35
38 (Y) REVERSE
29 A' 4-5
FILE BUS 4
8-7 34
FILE BUS 3
8-6 35
C4
C5


DA9
11 X1-R1-17F17
470
150
-2
B4
B4
6 10
A5 9-16 31
15
A5
A5
12 CAR5 23-29
B5
14
B5
B5
DA10
19 X1-R1-17F20
A6 9-17 32
25
A6
A6
20 CAR6 23-30
B6
24
B6
B6
21-35
38 (Y) REVERSE
B4
A4
29 A' 4-5
FILE BUS 3
B'
A5
D'
8-6 35
C4
C5
C5
33 E' 4-7
FILE BUS 2
B'
A6
D'
8-5 36
C5
C5
C OUT 7-6 41
13,14 C OUT 7-5 42
18
D6 DIFF 2
7-17-71


3 DA11 XI-RI-16F3
A7 9-18 30
470
150
-2
2I-16
39 SET ADDRESS
5
A7
A7
4 CAR 7 23-31
B7
4
B7
B7
21-15
CLEAR
40 ADDRESS
11 DA12 XI-RI-16F5
A8 9-19 31
15
A8
A8 19-6 13
12 CAR 8 23-32
B8
14
B8
B8
DA13
19 XI-RI-16F10
A9
32
28 READ FF 13-30
25 B' 4-6
27 D' 4-3
5 C IN 6-42
6 C IN 6-41
21-34
37 (X) FORWARD
21-35
38 (Y) REVERSE
26 C' 4-4
29 FORWARD 21-34
33 WRITE FF 14-6
FILE BUS I
8-4 34
470
-2
FILE BUS 0
8-3 35
470
-2
A7
B7
A8
B8
C7
C8



D7 DIFF 3

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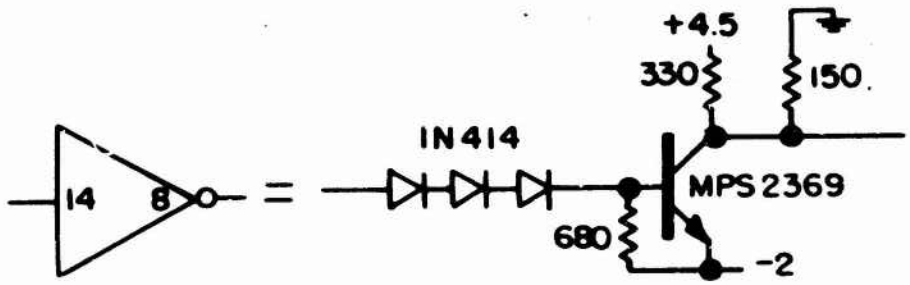
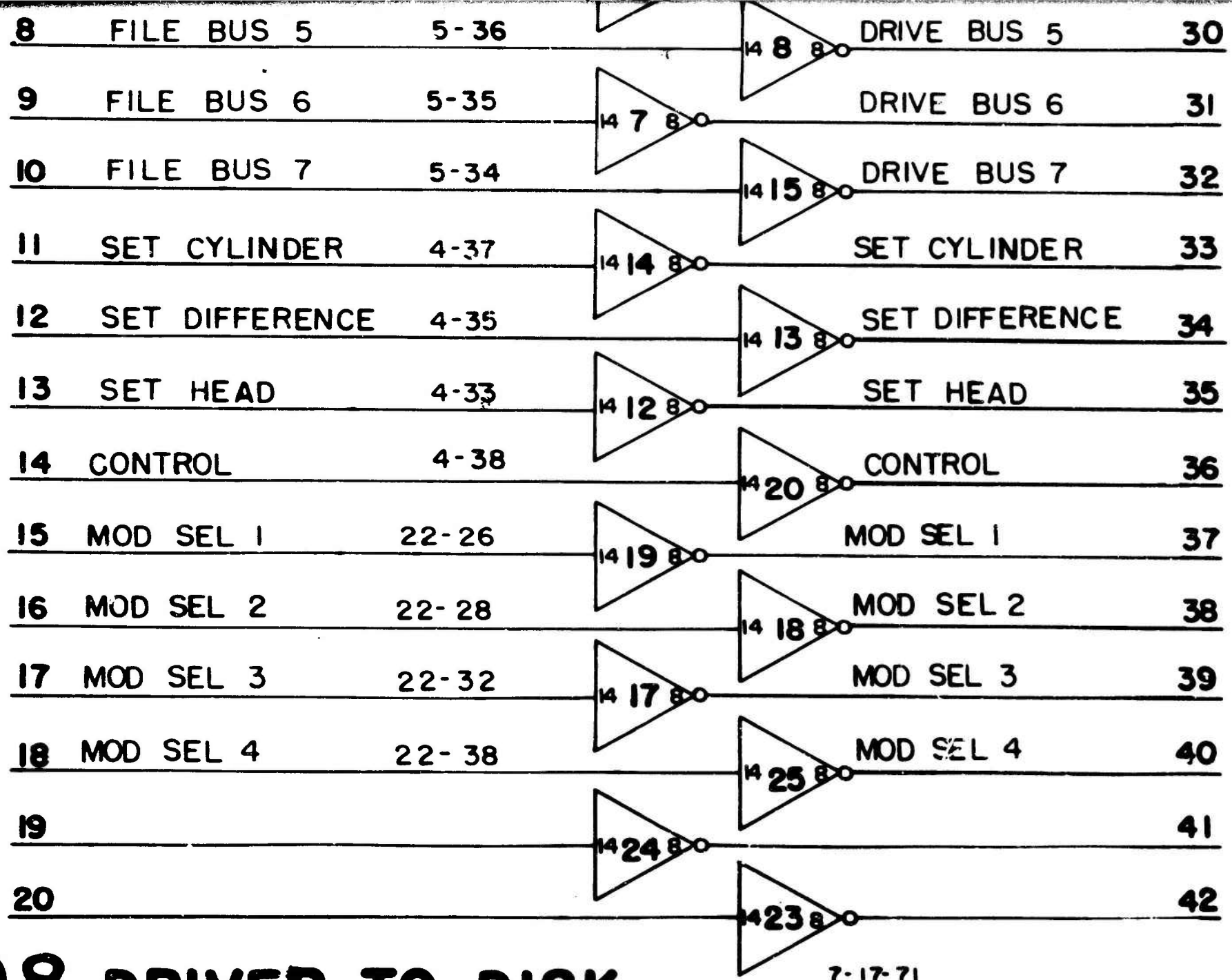
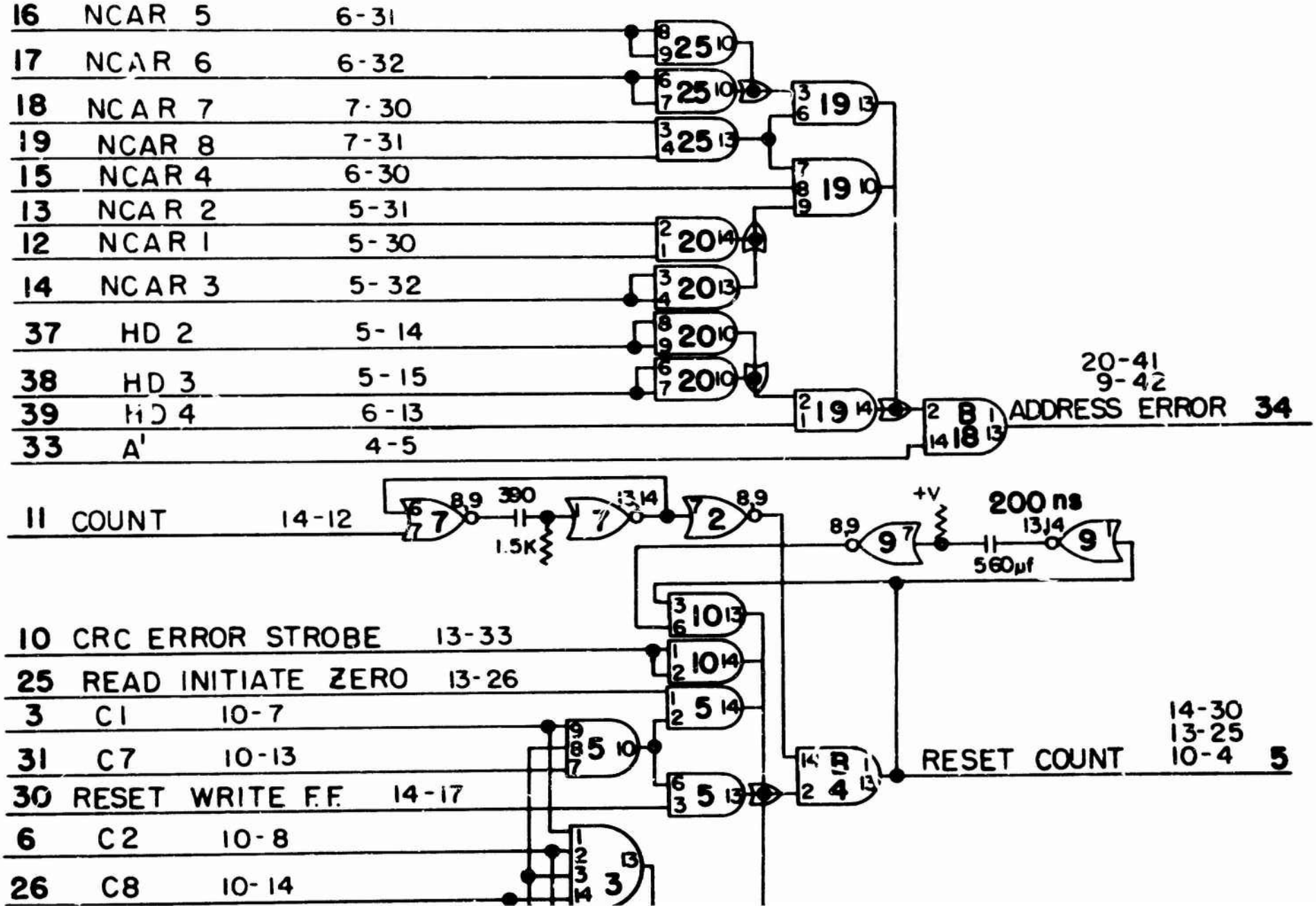


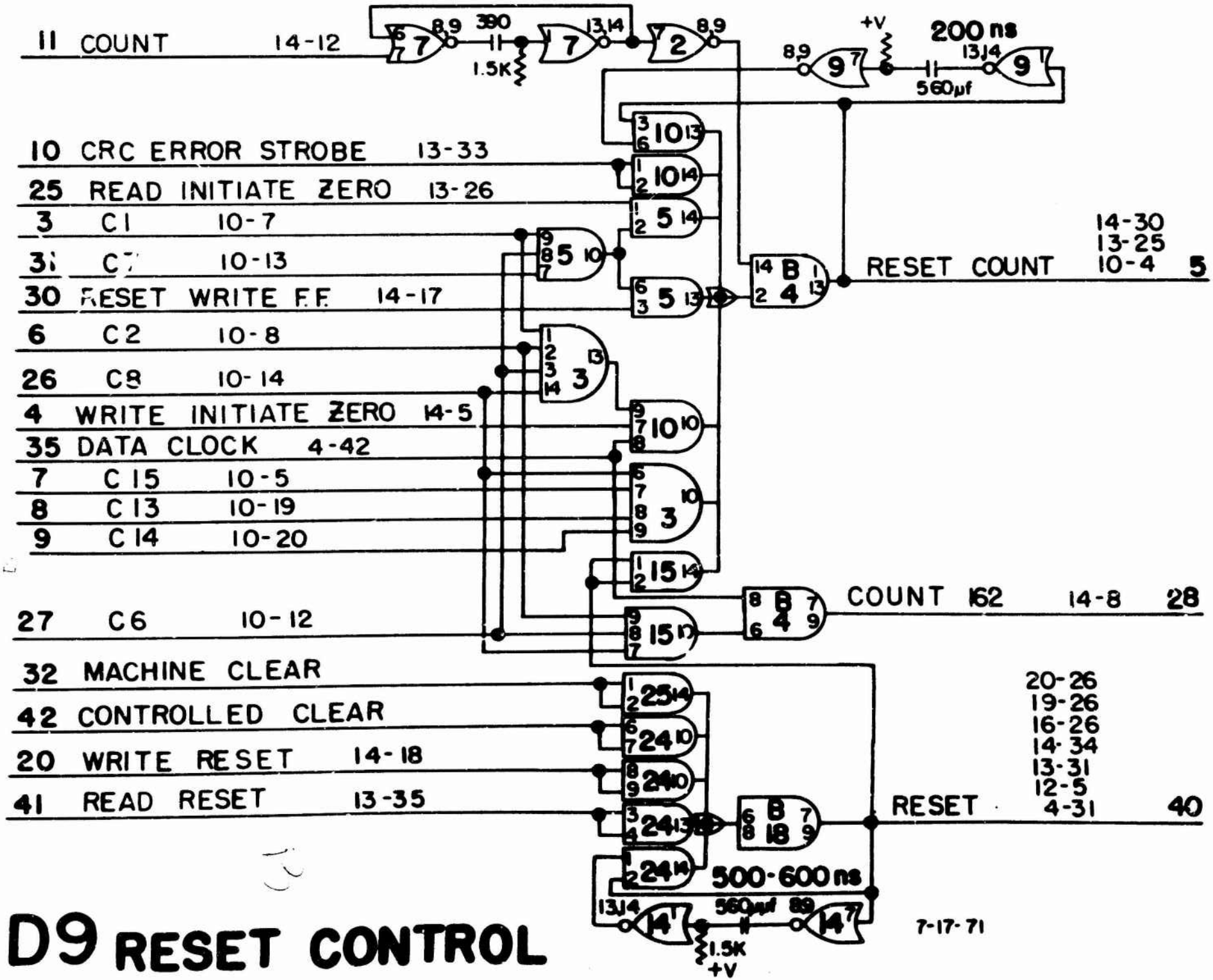
3	FILE BUS 0	7 35	14 5 8	DRIVE BUS 0	25
4	FILE BUS 1	7-34	14 4 8	DRIVE BUS 1	26
5	FILE BUS 2	6-36	14 3 8	DRIVE BUS 2	27
6	FILE BUS 3	6-35	14 10 8	DRIVE BUS 3	28
7	FILE BUS 4	6-34	14 9 8	DRIVE BUS 4	29
8	FILE BUS 5	5-36	14 8 8	DRIVE BUS 5	30
9	FILE BUS 6	5-35	14 7 8	DRIVE BUS 6	31
10	FILE BUS 7	5-34	14 15 8	DRIVE BUS 7	32
11	SET CYLINDER	4-37	14 14 8	SET CYLINDER	33
12	SET DIFFERENCE	4-35	14 13 8	SET DIFFERENCE	34
13	SET HEAD	4-33	14 12 8	SET HEAD	35



D8 DRIVER TO DISK

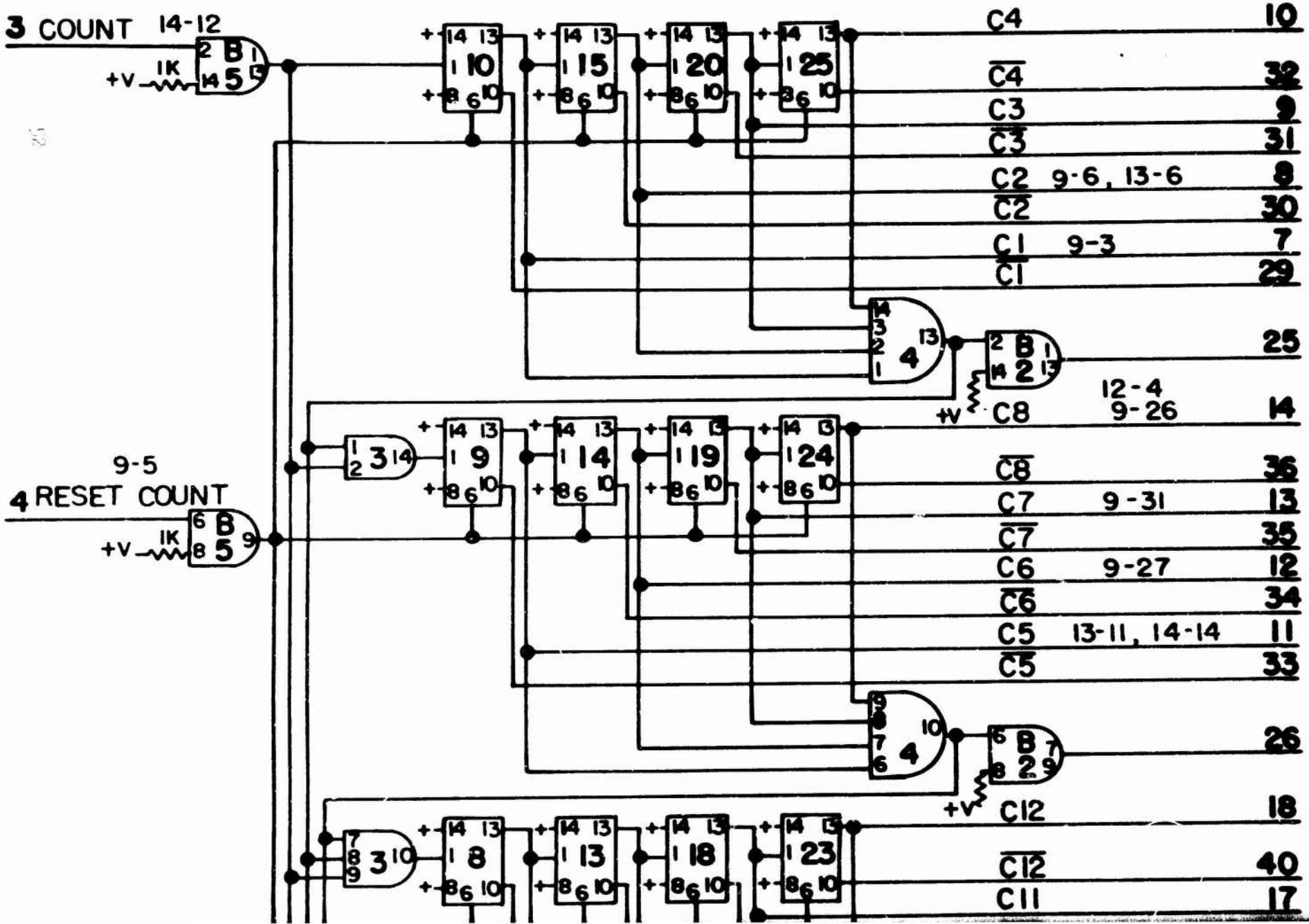
7-17-71

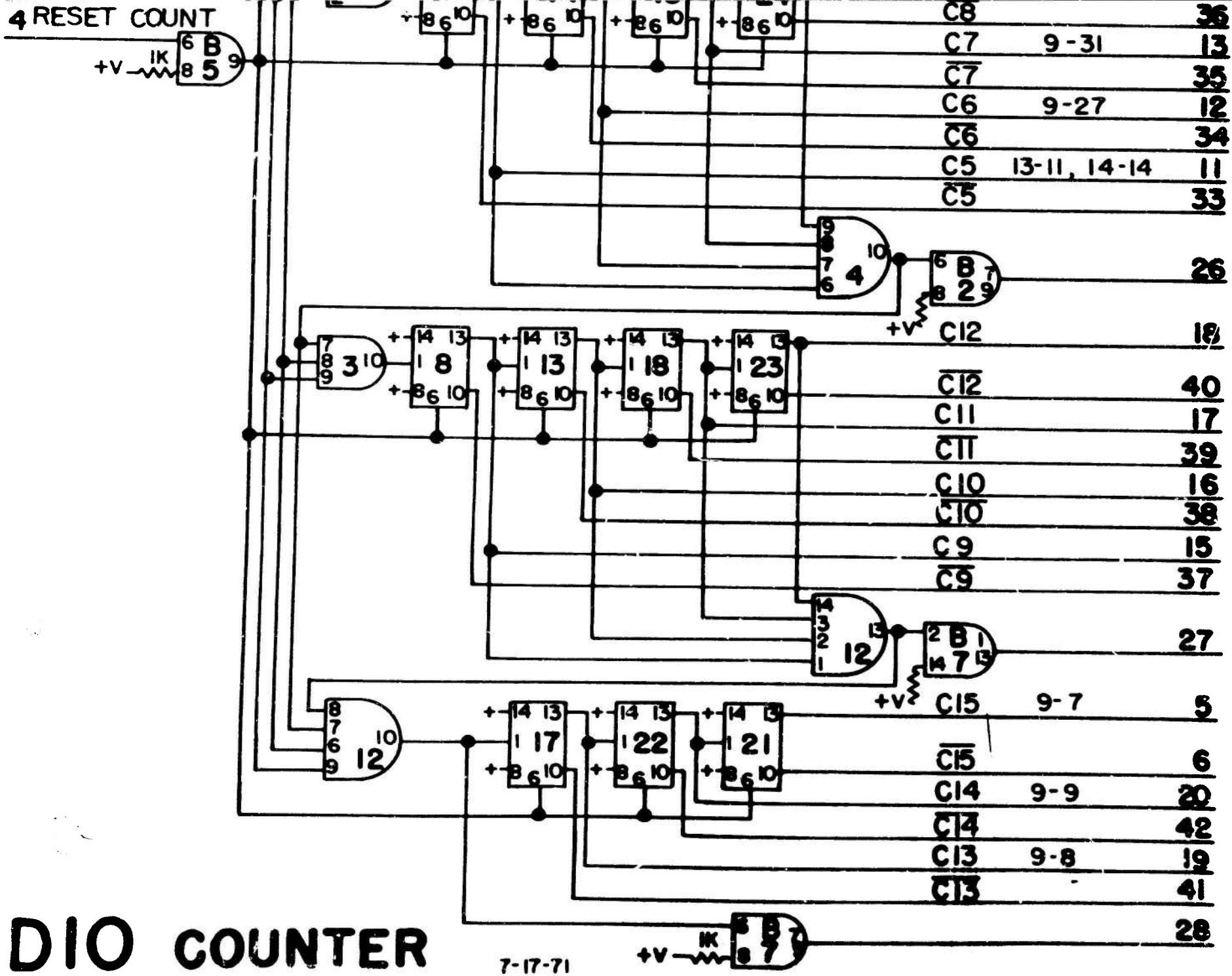

16 NCAR 5 6-31
17 NCAR 6 6-32
18 NCAR 7 7-30
19 NCAR 8 7-31
15 NCAR 4 6-30
13 NCAR 2 5-31
12 NCAR 1 5-30
14 NCAR 3 5-32
37 HD 2 5-14
38 HD 3 5-15
39 HD 4 6-13
33 A' 4-5
20-41
9-42
ADDRESS ERROR 34
11 COUNT 14-12
390
1.5K
+V
200 ns
560µf
10 CRC ERROR STROBE 13-33
25 READ INITIATE ZERO 13-26
3 C1 10-7
31 C7 10-13
30 RESET WRITE F.F. 14-17
6 C2 10-8
26 C8 10-14
14-30
13-25
10-4 5
RESET COUNT



D9 RESET CONTROL

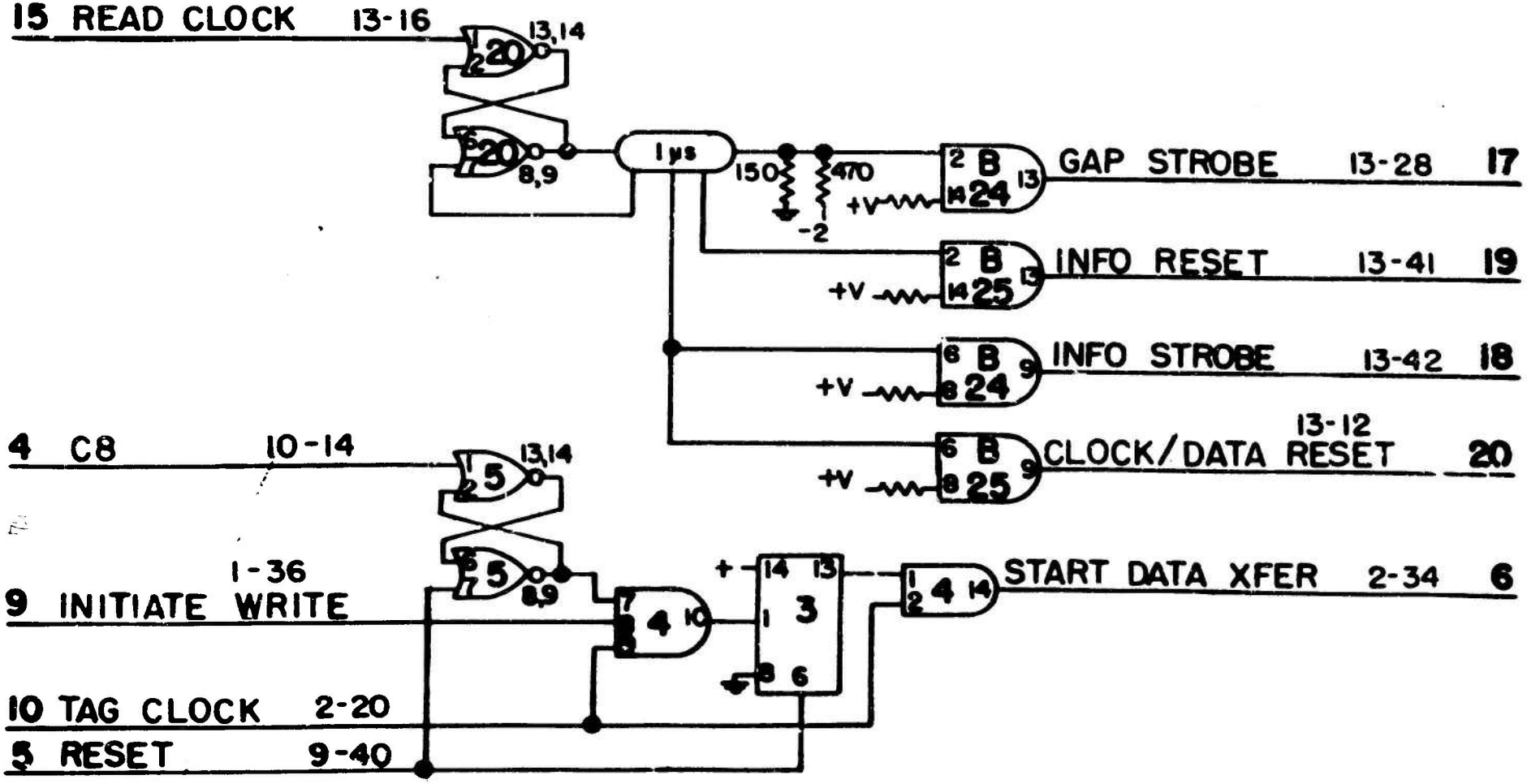
7-17-71


3 COUNT 14-12
+V
1K
C4
10
C4
32
C3
9
C3
31
C2
9-6, 13-6
8
C2
30
C1
9-3
7
C1
29
25
+V
C8
12-4
9-26
14
9-5
4 RESET COUNT
+V
1K
C8
36
C7
9-31
13
C7
35
C6
9-27
12
C6
34
C5
13-11, 14-14
11
C5
33
26
+V
C12
18
C12
40
C11
17



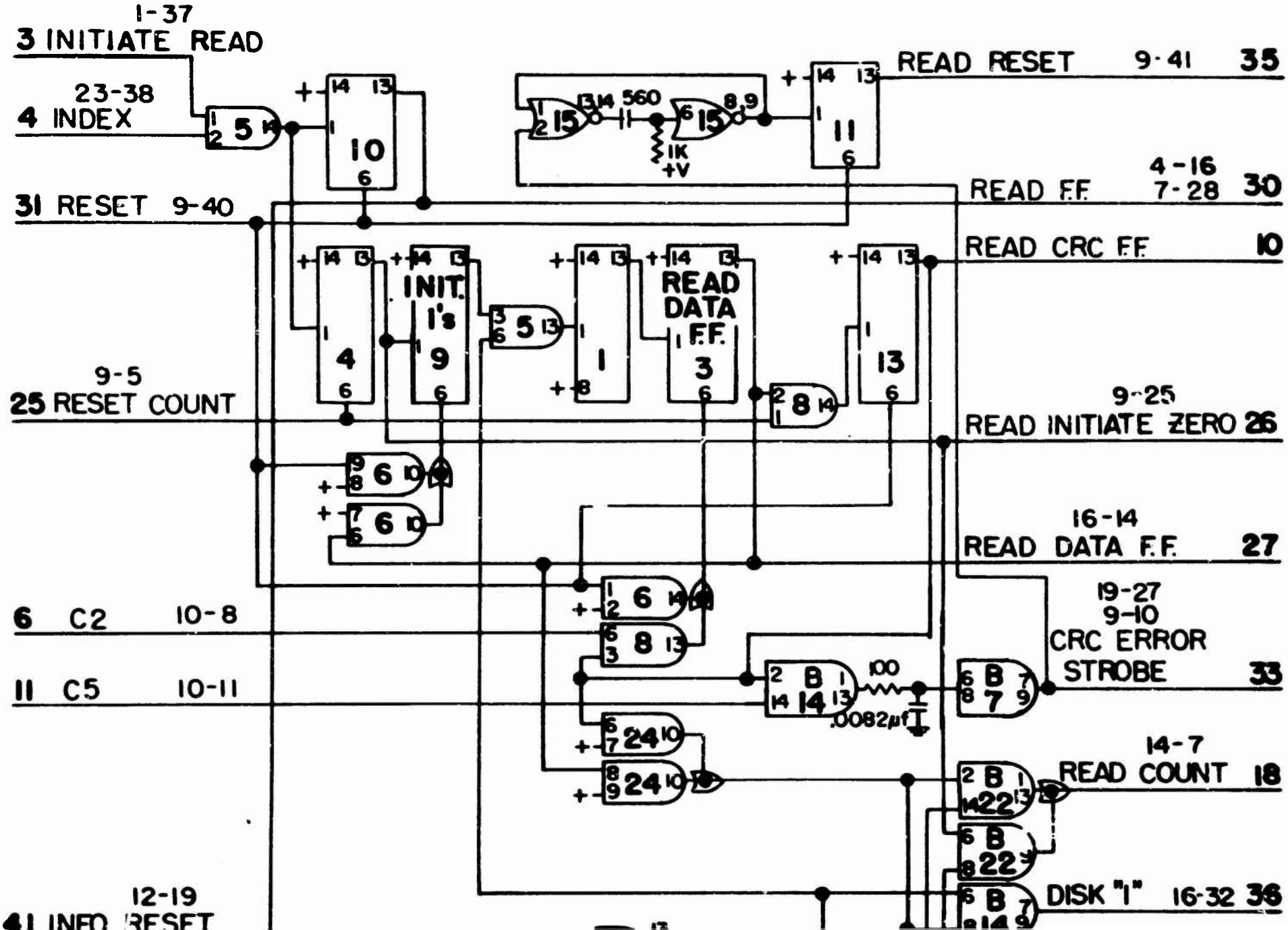
DIO COUNTER

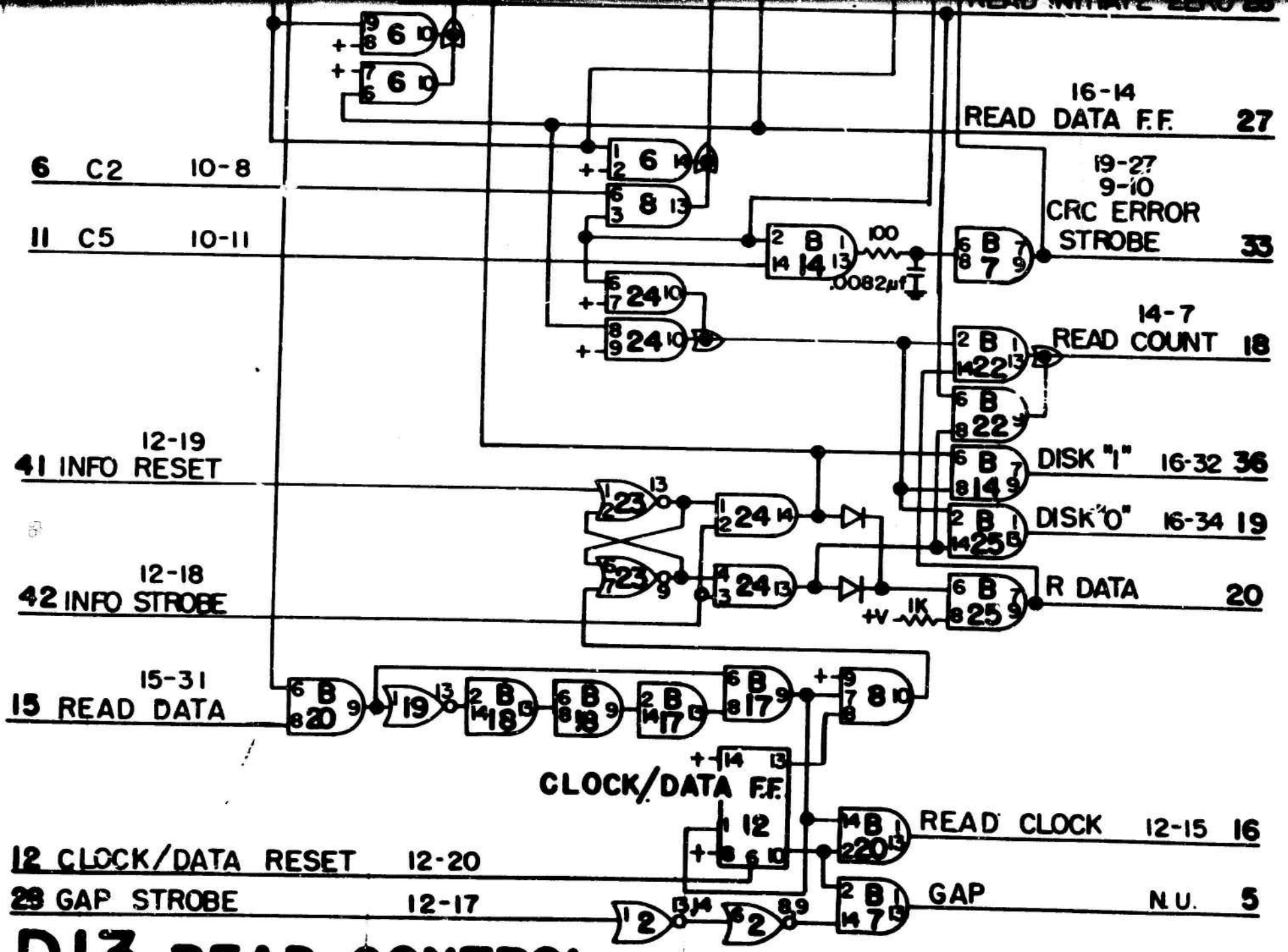
7-17-71



D12 DELAY LINE

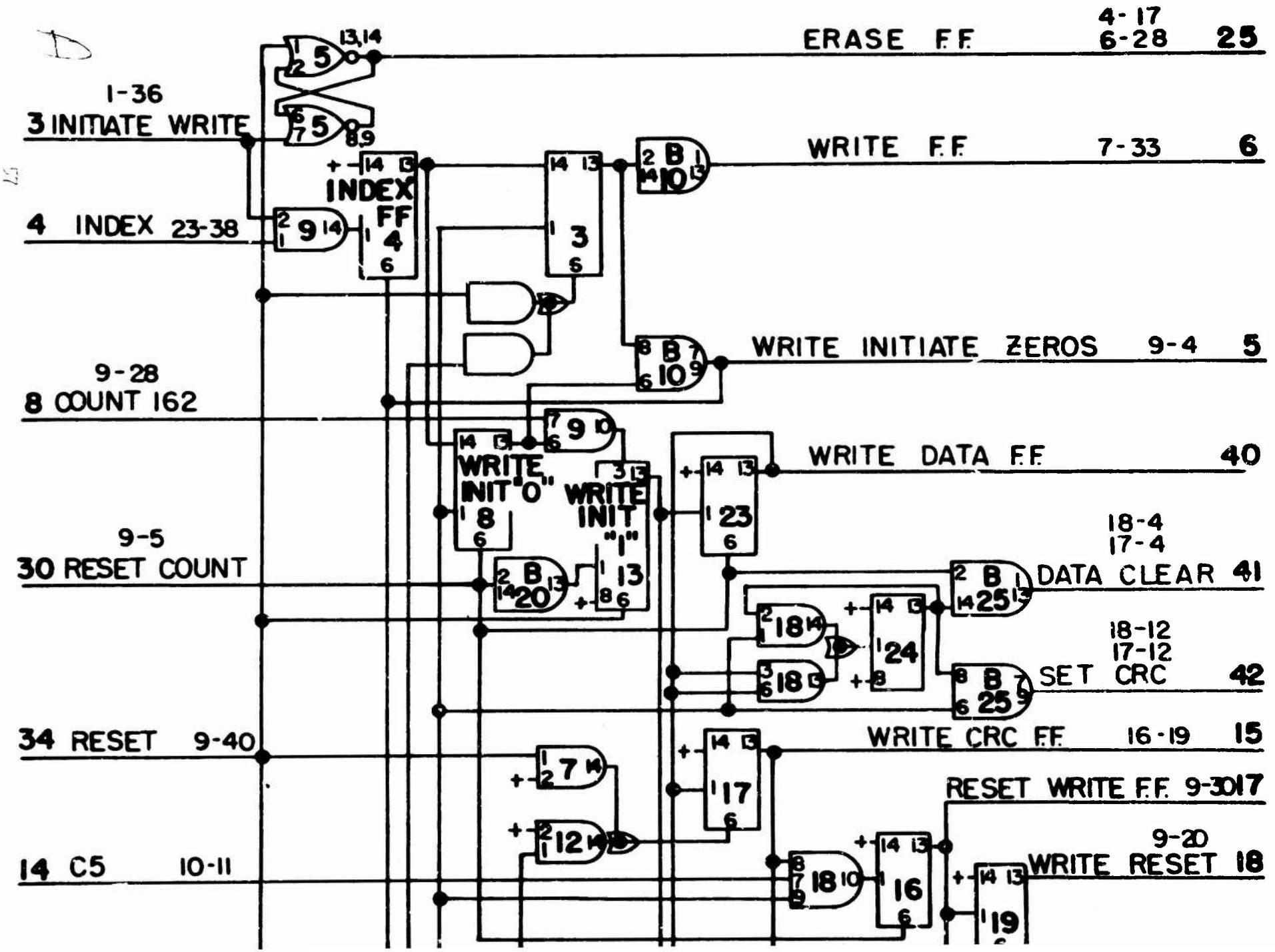
7-16-71

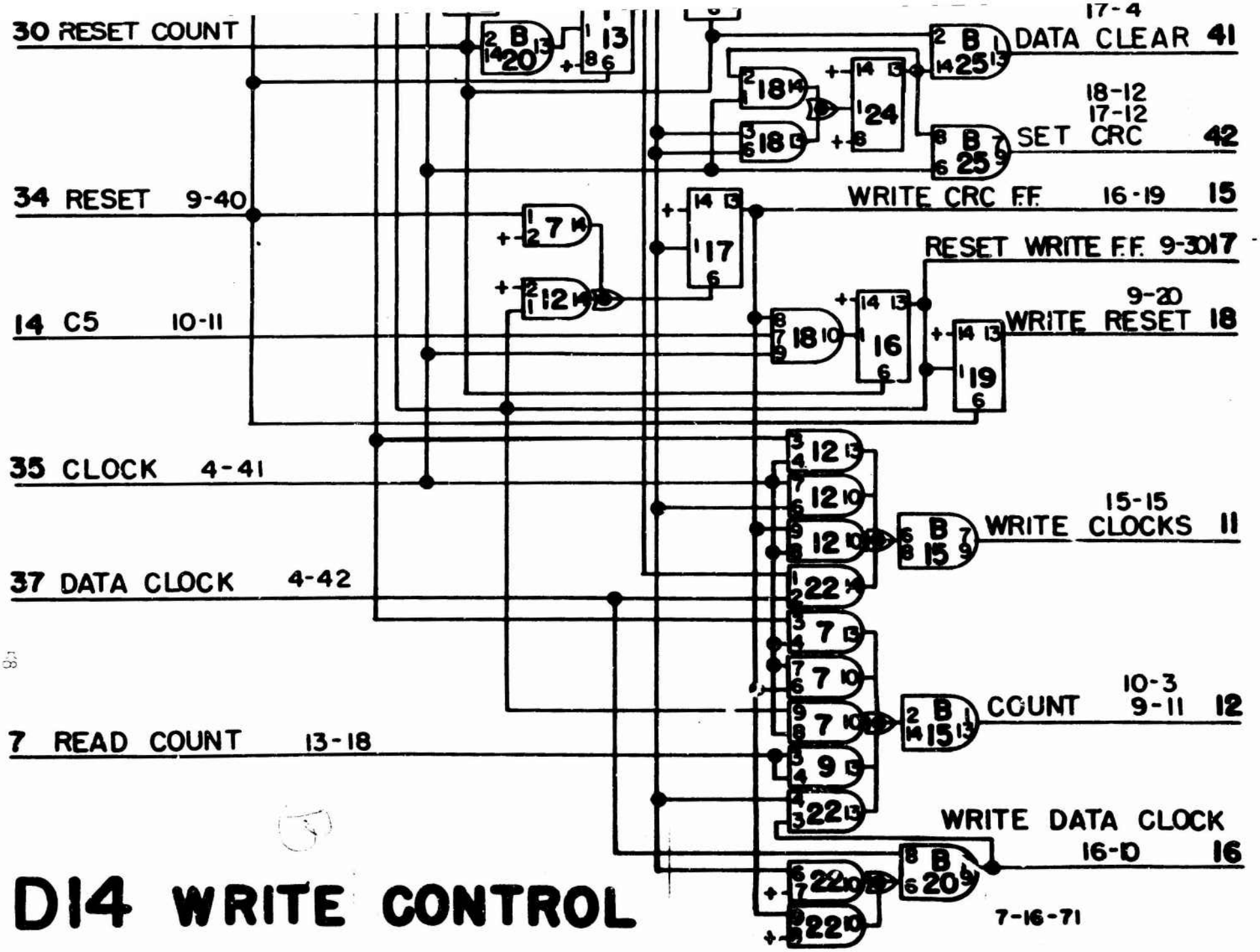

1-37
3 INITIATE READ
23-38
4 INDEX
31 RESET 9-40
9-5
25 RESET COUNT
6 C2 10-8
11 C5 10-11
12-19
41 UNFD RESET
INIT. 1's
READ DATA F.F.
560
1K
+V
100
.0082μf
READ RESET 9-41 35
4-16
READ F.F. 7-28 30
READ CRC F.F. 10
9-25
READ INITIATE ZERO 26
16-14
READ DATA F.F. 27
19-27
9-10
CRC ERROR STROBE 33
14-7
READ COUNT 18
DISK "1" 16-32 36



D13 READ CONTROL

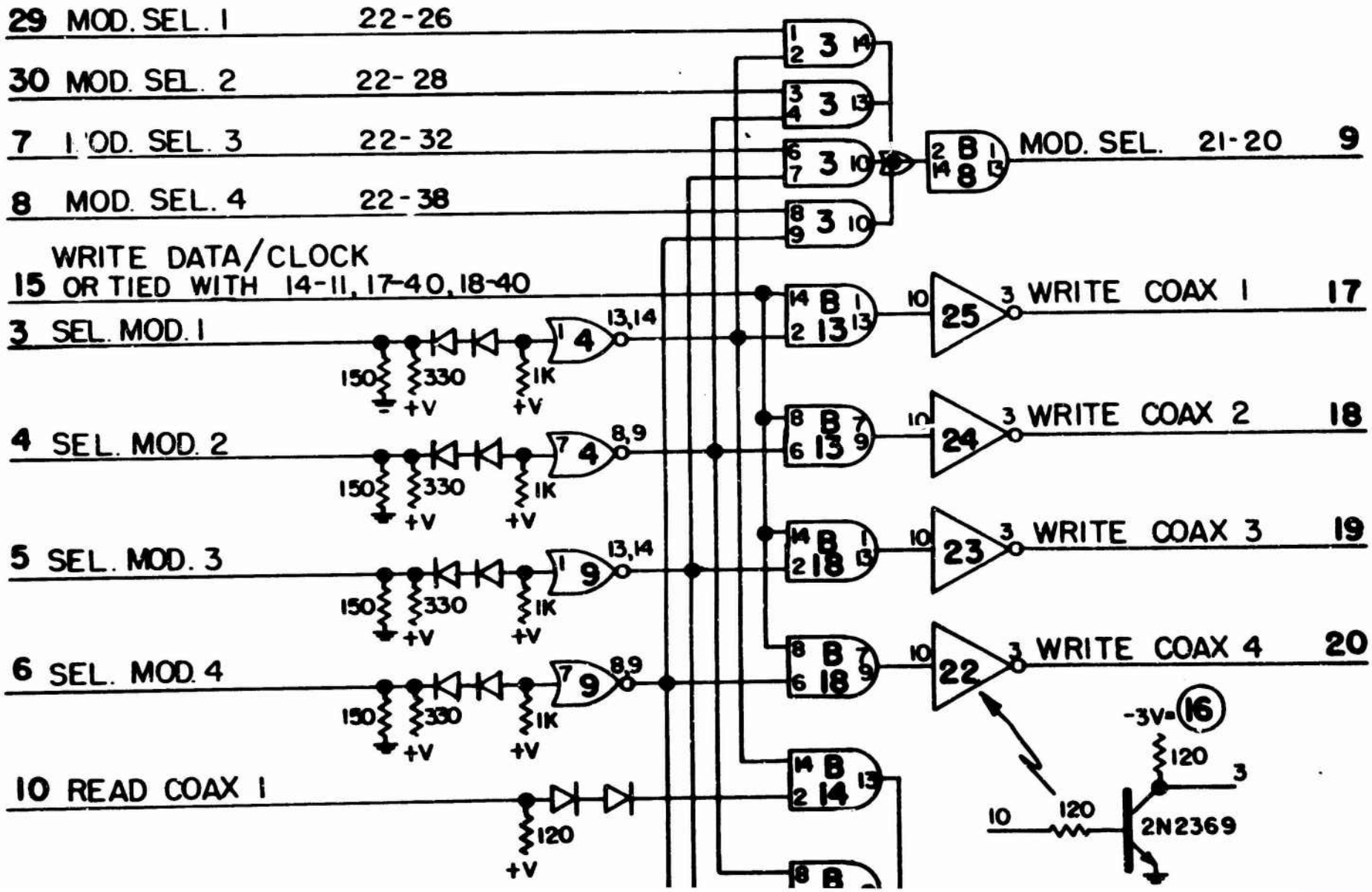
7-16-71

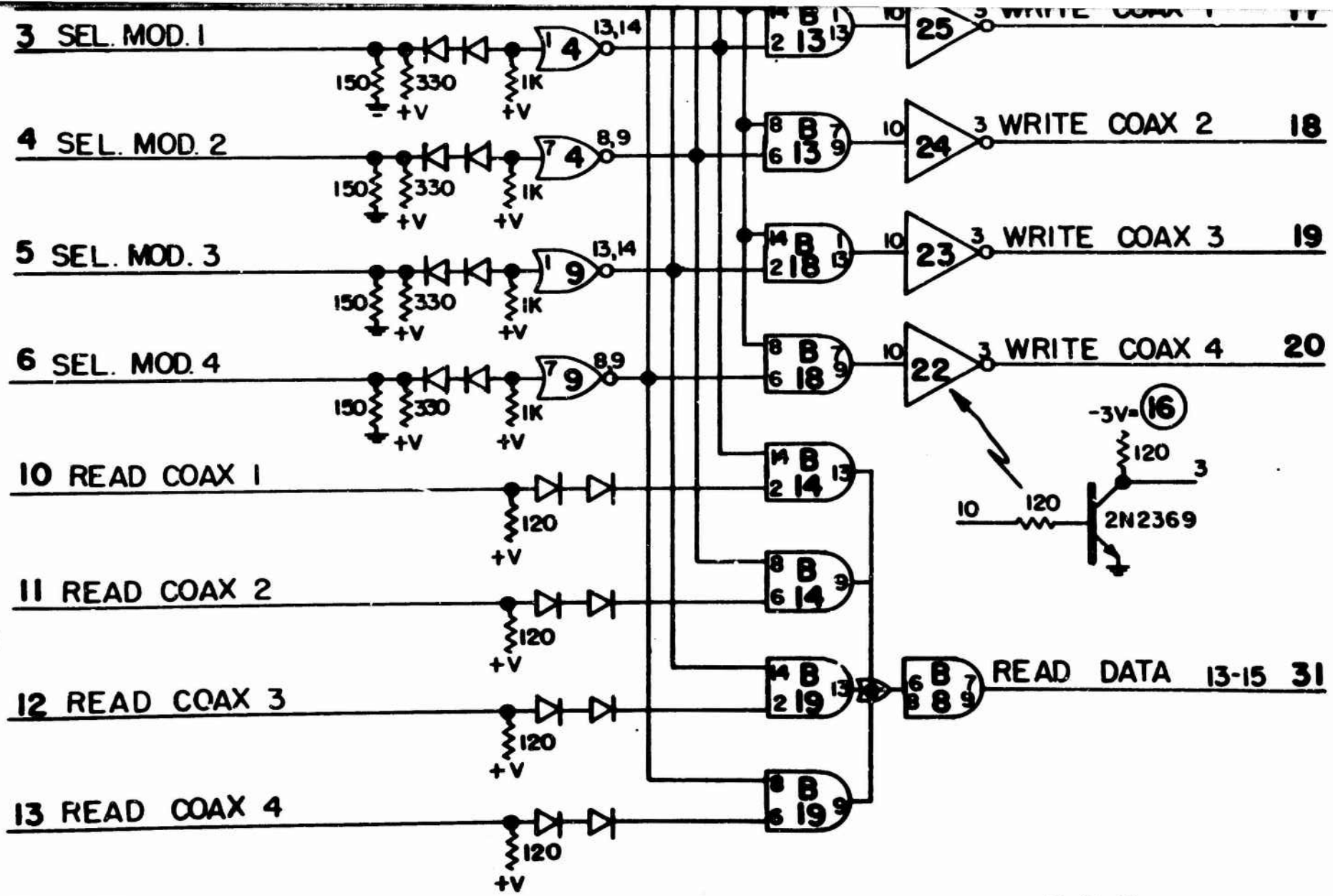

ERASE F.F.
4-17
6-28
25
1-36
3 INITIATE WRITE
WRITE F.F.
7-33
6
INDEX FF
4 INDEX 23-38
WRITE INITIATE ZEROS
9-4
5
9-28
8 COUNT 162
WRITE INIT "0"
WRITE INIT "1"
WRITE DATA F.F.
40
9-5
30 RESET COUNT
18-4
17-4
DATA CLEAR
41
18-12
17-12
SET CRC
42
34 RESET 9-40
WRITE CRC F.F.
16-19
15
RESET WRITE F.F. 9-30
17
14 C5 10-11
9-20
WRITE RESET
18



D14 WRITE CONTROL

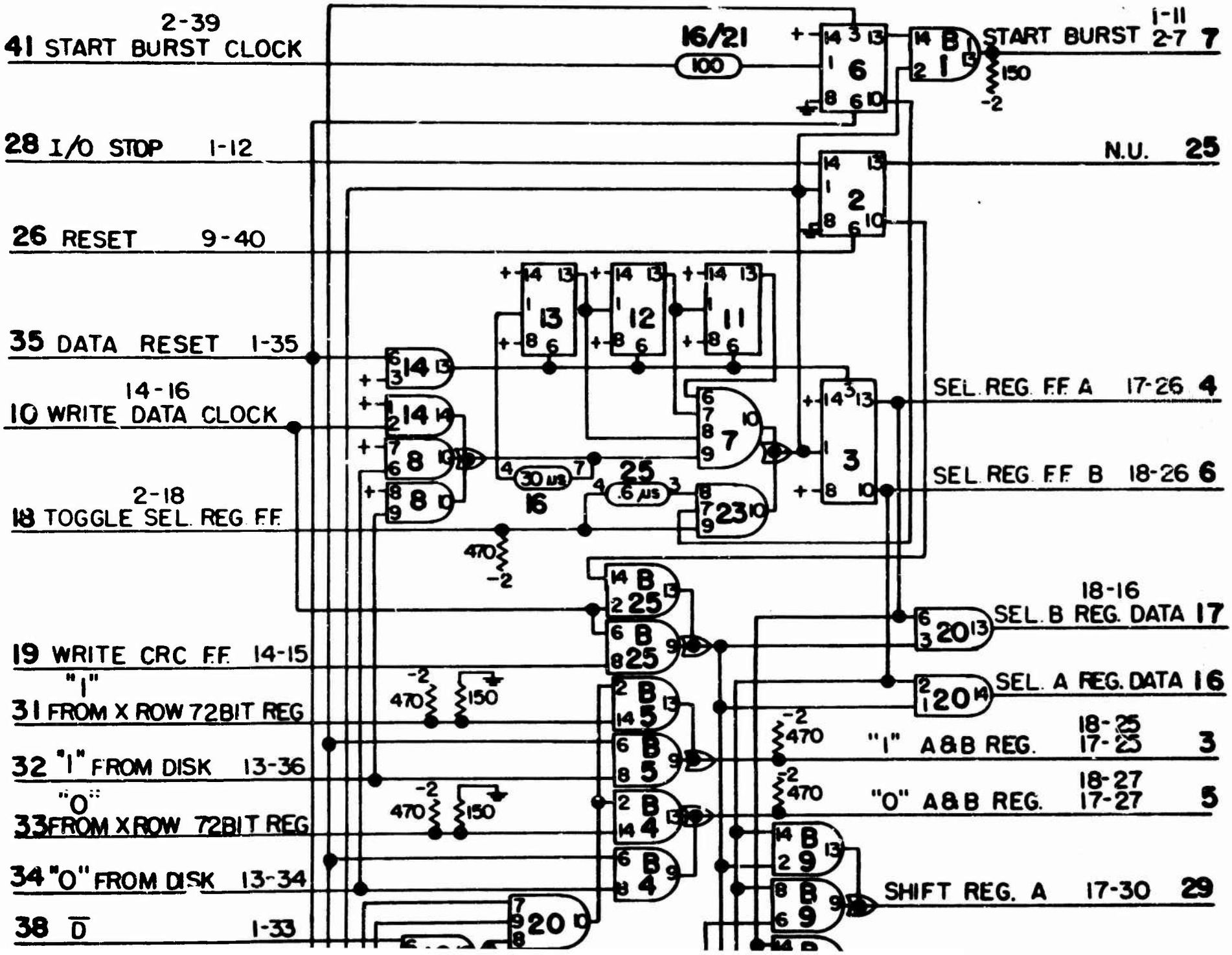
7-16-71

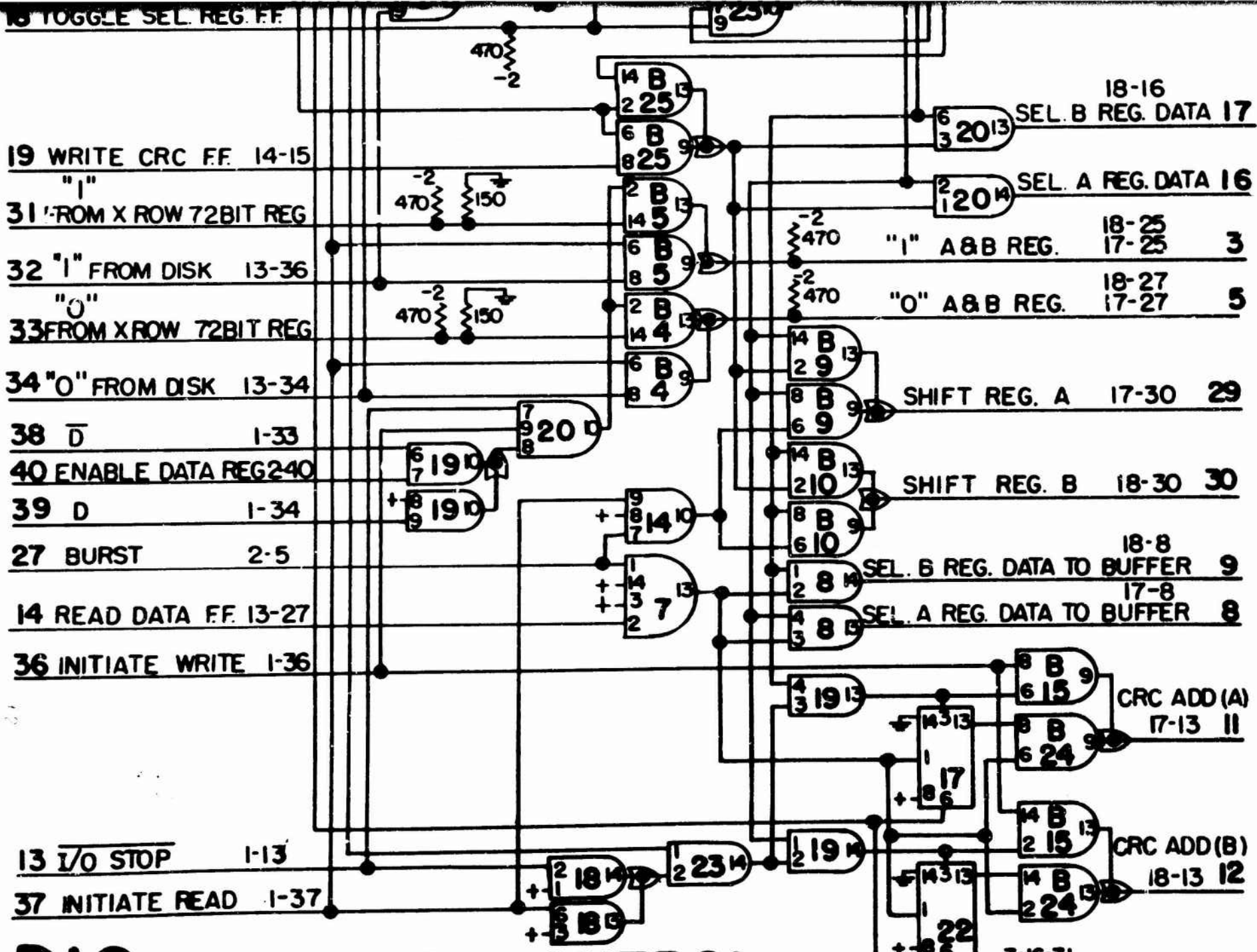

29 MOD. SEL. 1 22-26
30 MOD. SEL. 2 22-28
7 MOD. SEL. 3 22-32
8 MOD. SEL. 4 22-38
WRITE DATA/CLOCK
15 OR TIED WITH 14-11, 17-40, 18-40
3 SEL. MOD. 1
4 SEL. MOD. 2
5 SEL. MOD. 3
6 SEL. MOD. 4
10 READ COAX 1
150
330
1K
120
+V
MOD. SEL. 21-20 9
WRITE COAX 1 17
WRITE COAX 2 18
WRITE COAX 3 19
WRITE COAX 4 20
-3V
16
2N2369



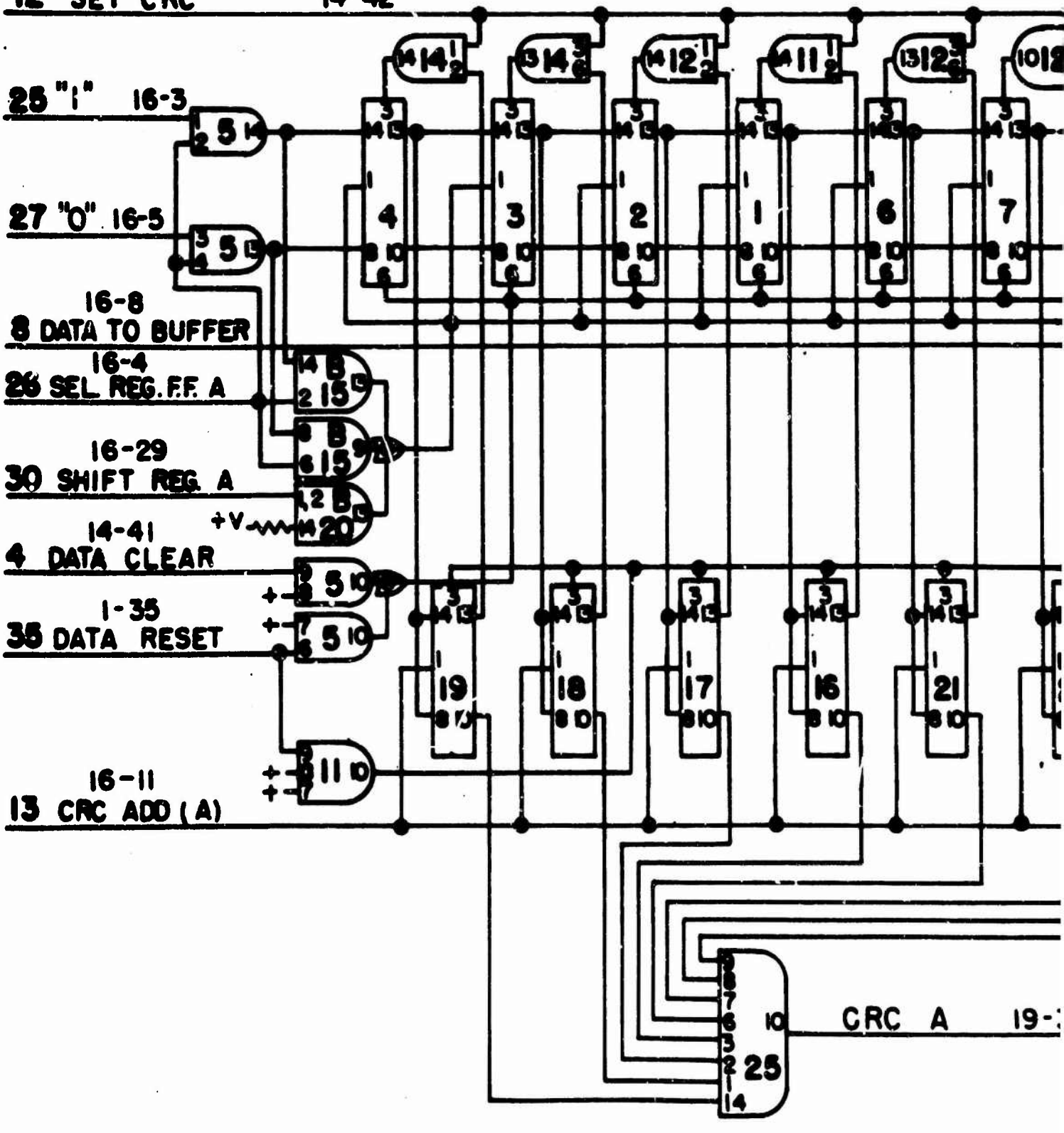
D15 READ & WRITE INTERFACE

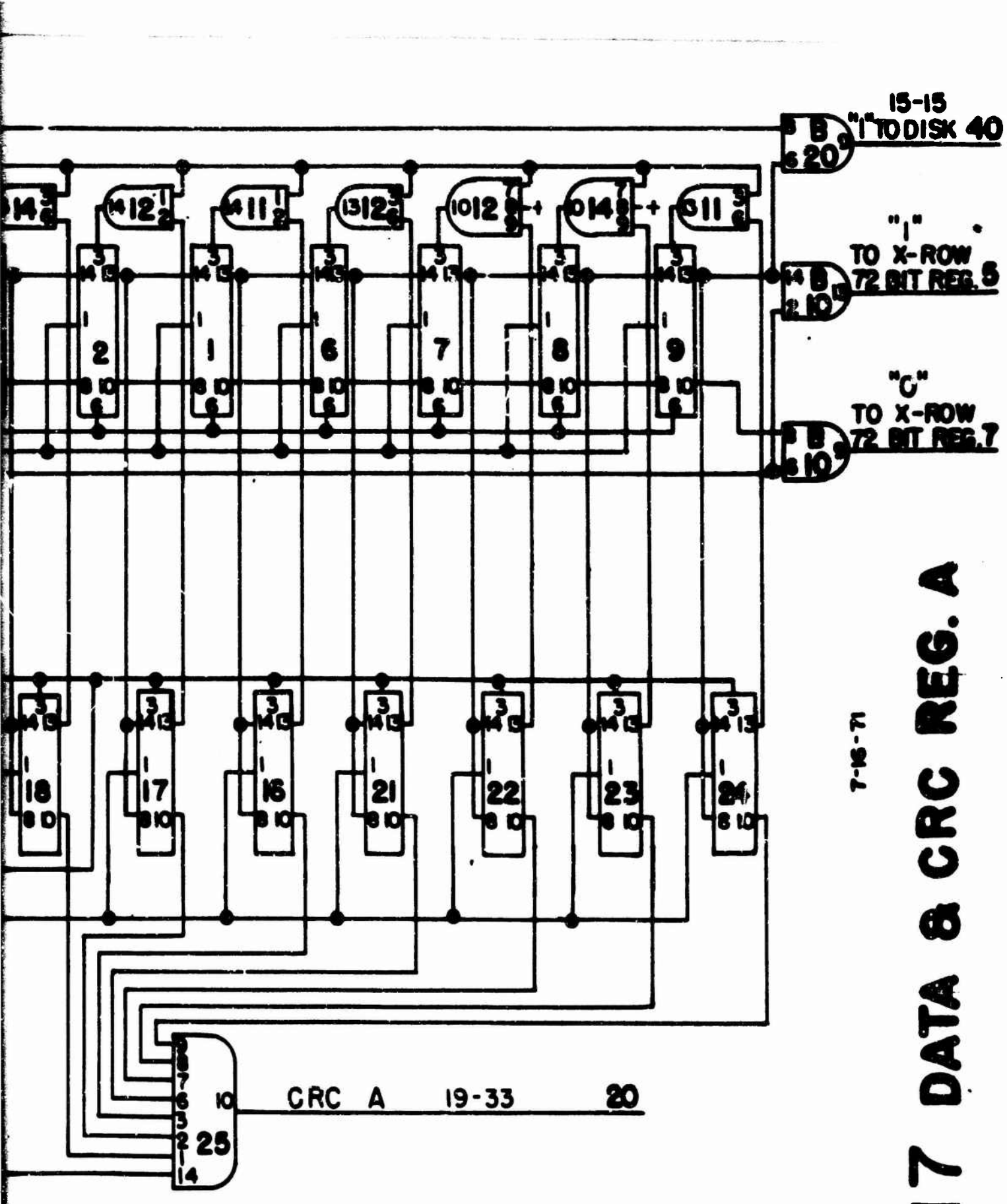
7-16-71


2-39
41 START BURST CLOCK
28 I/O STOP 1-12
26 RESET 9-40
35 DATA RESET 1-35
14-16
10 WRITE DATA CLOCK
2-18
18 TOGGLE SEL. REG F.F.
19 WRITE CRC F.F. 14-15
"1"
31 FROM X ROW 72BIT REG
32 "1" FROM DISK 13-36
"0"
33 FROM X ROW 72BIT REG
34 "0" FROM DISK 13-34
38 D 1-33
16/21
100
START BURST 1-11 2-7 7
150
-2
N.U. 25
SEL. REG. F.F. A 17-26 4
SEL. REG. F.F. B 18-26 6
30 µs
16
25
.6 µs
470
18-16
SEL. B REG. DATA 17
SEL. A REG. DATA 16
"1" A&B REG. 18-25 17-25 3
"0" A&B REG. 18-27 17-27 5
SHIFT REG. A 17-30 29

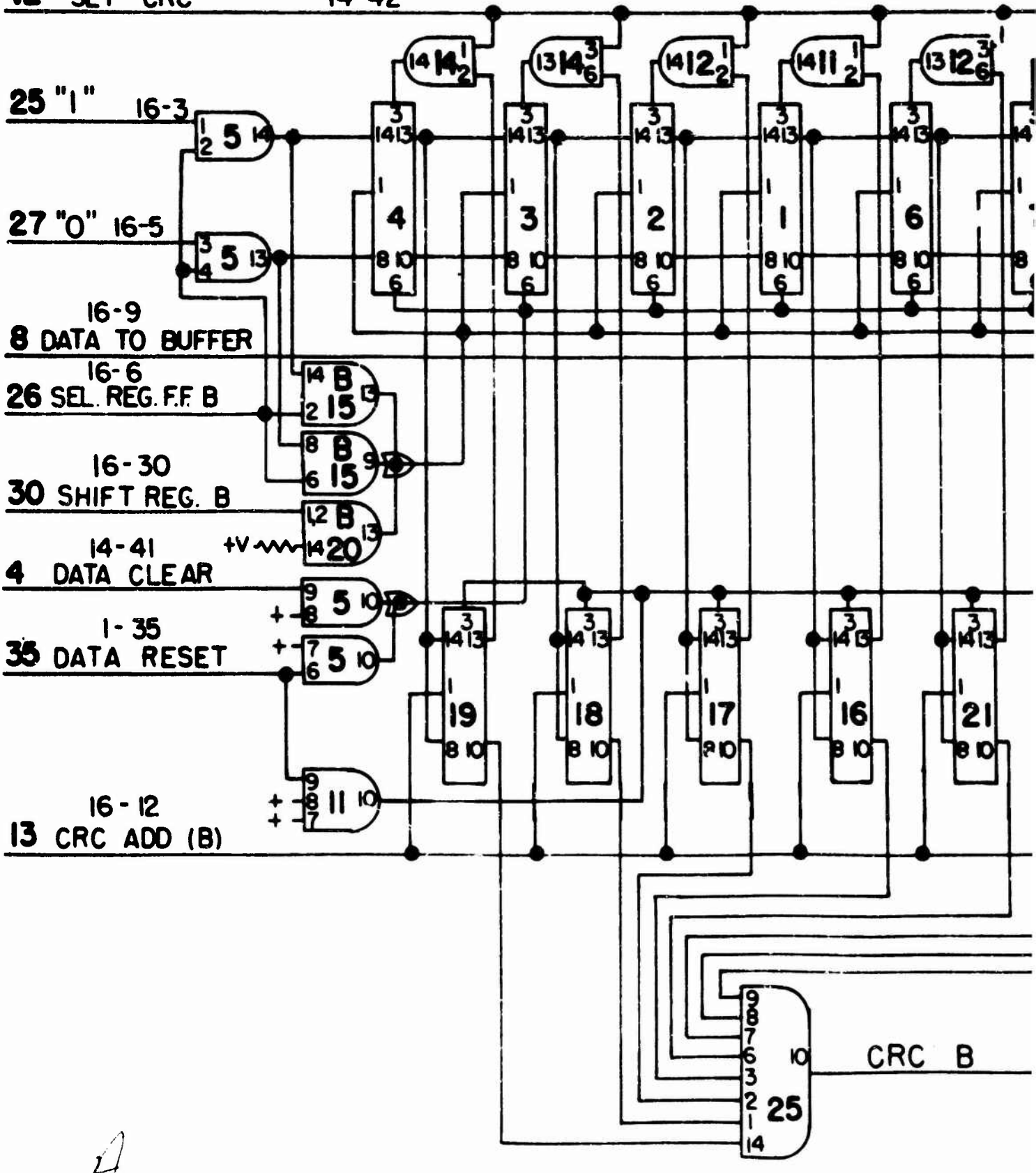


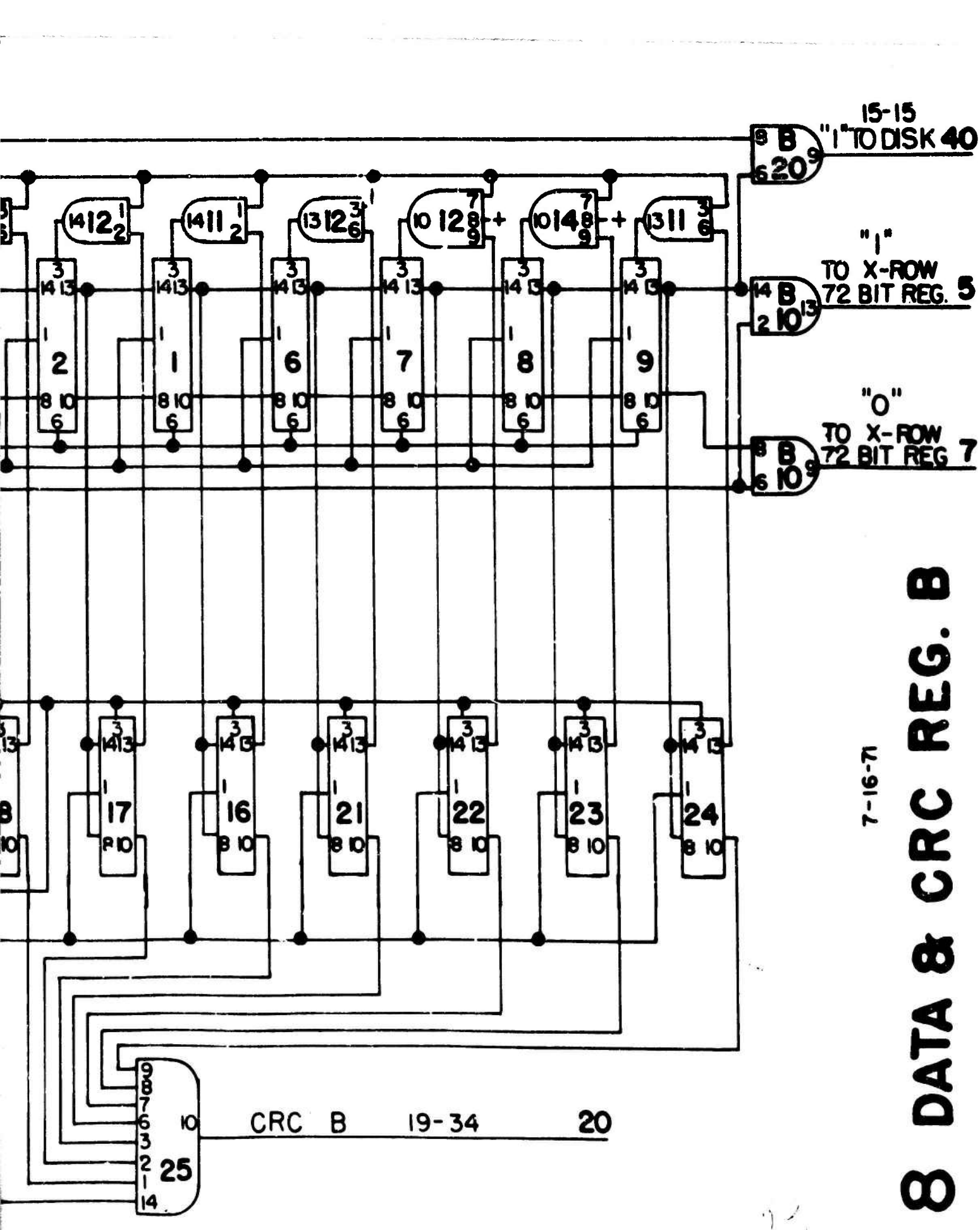
D16 REGISTER CONTROL


16 DATA TO DISK 16-16
12 SET CRC 14-42
25 "1" 16-3
27 "0" 16-5
16-8
8 DATA TO BUFFER
16-4
26 SEL. REG. F.F. A
16-29
30 SHIFT REG. A
+V
14-41
4 DATA CLEAR
1-35
35 DATA RESET
16-11
13 CRC ADD (A)
CRC A 19-
4
3
2
1
6
7
19
18
17
16
21
25



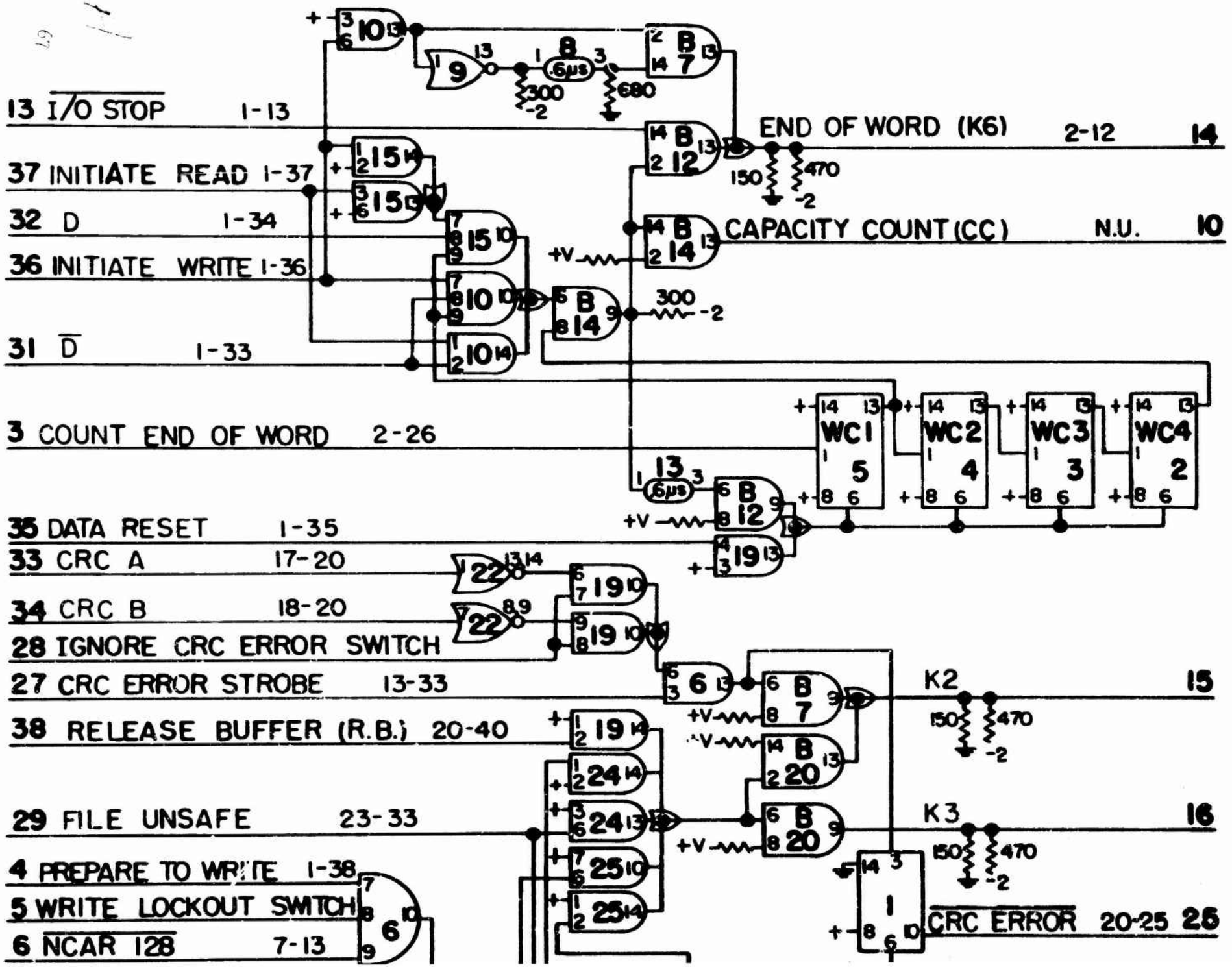
D17 DATA & CRC REG. A

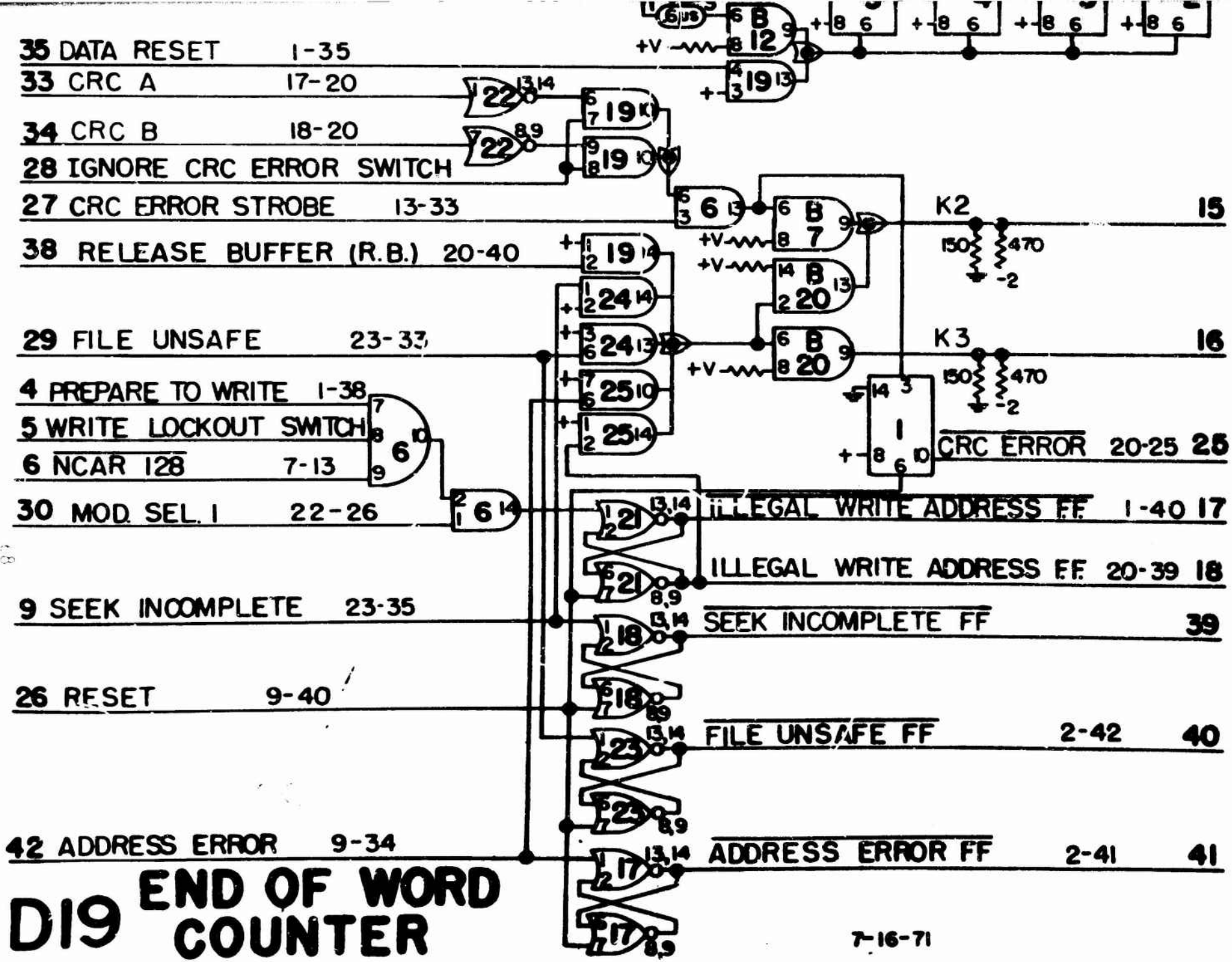

16 DATA TO DISK 16-17
12 SET CRC 14-42
25 "1" 16-3
27 "0" 16-5
16-9
8 DATA TO BUFFER
16-6
26 SEL. REG. F.F. B
16-30
30 SHIFT REG. B
14-41
4 DATA CLEAR
1-35
35 DATA RESET
16-12
13 CRC ADD (B)
+V
CRC B



D18 DATA & CRC REG. B

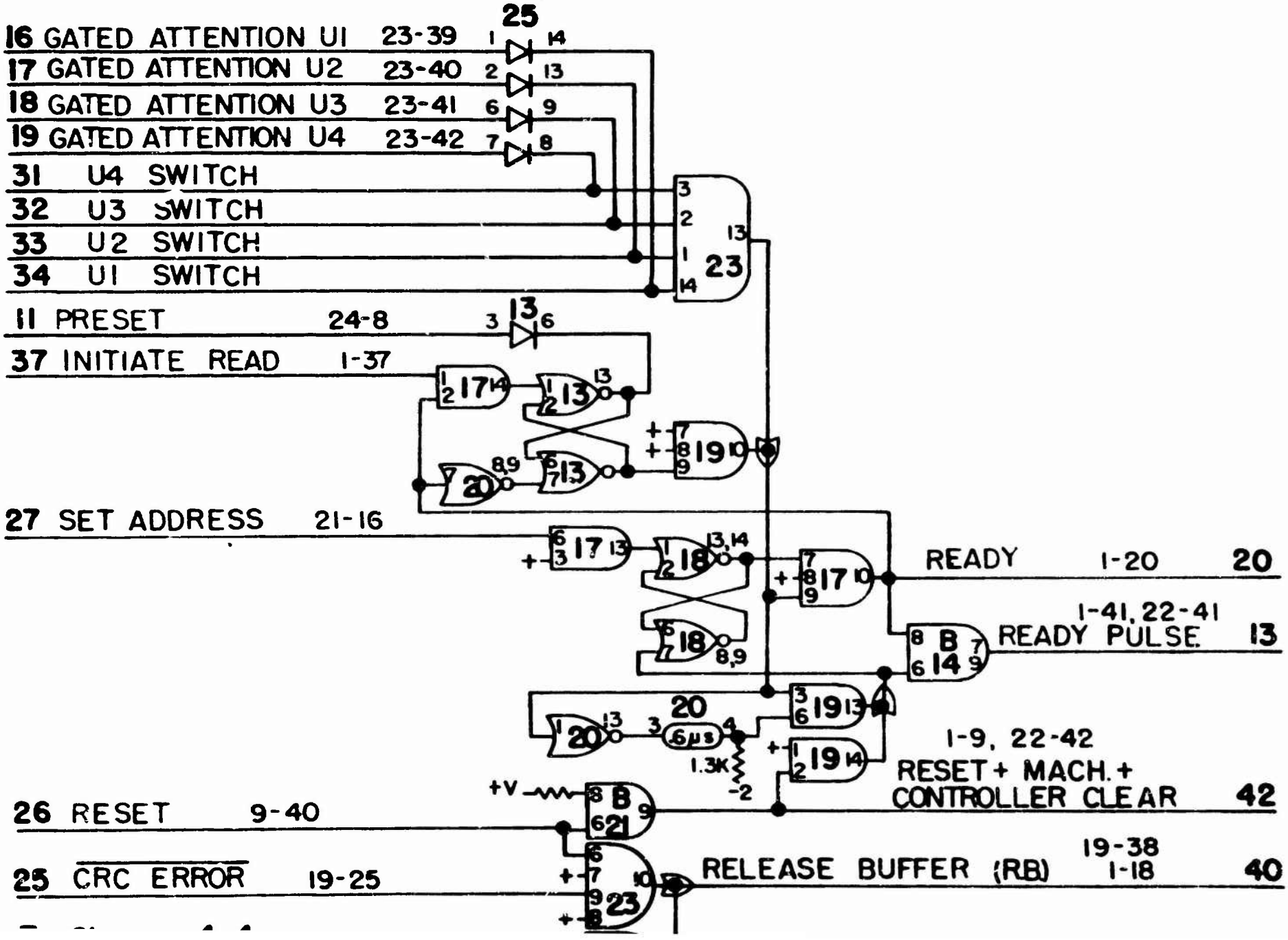
7-16-71

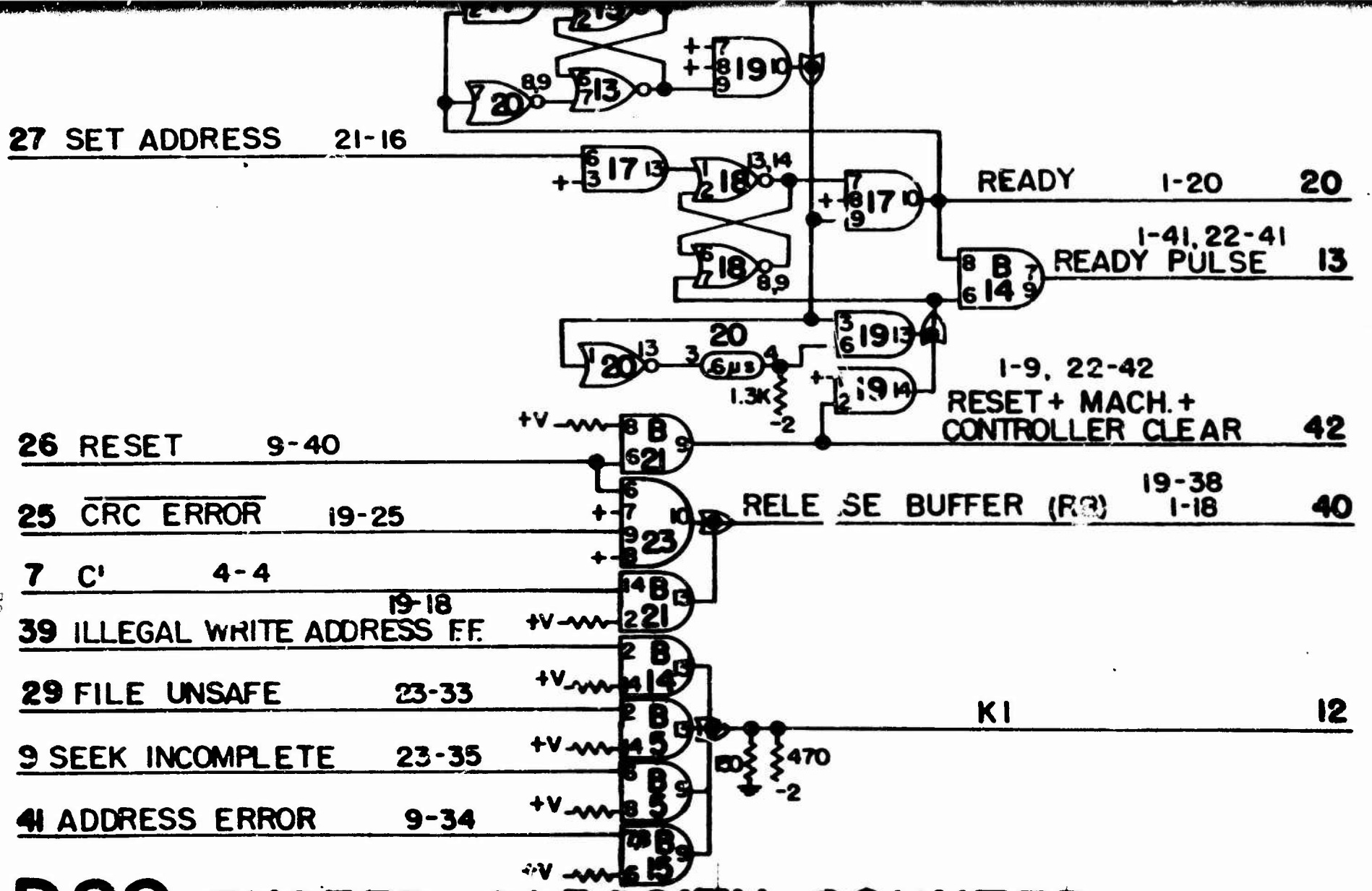

13 I/O STOP 1-13
37 INITIATE READ 1-37
32 D 1-34
36 INITIATE WRITE 1-36
31 D 1-33
3 COUNT END OF WORD 2-26
35 DATA RESET 1-35
33 CRC A 17-20
34 CRC B 18-20
28 IGNORE CRC ERROR SWITCH
27 CRC ERROR STROBE 13-33
38 RELEASE BUFFER (R.B.) 20-40
29 FILE UNSAFE 23-33
4 PREPARE TO WRITE 1-38
5 WRITE LOCKOUT SWITCH
6 NCAR 128 7-13
END OF WORD (K6) 2-12 14
CAPACITY COUNT (CC) N.U. 10
K2 15
K3 16
CRC ERROR 20-25 25
WC1
WC2
WC3
WC4
+V
300
-2
150
470
680
6µs



D19 END OF WORD COUNTER

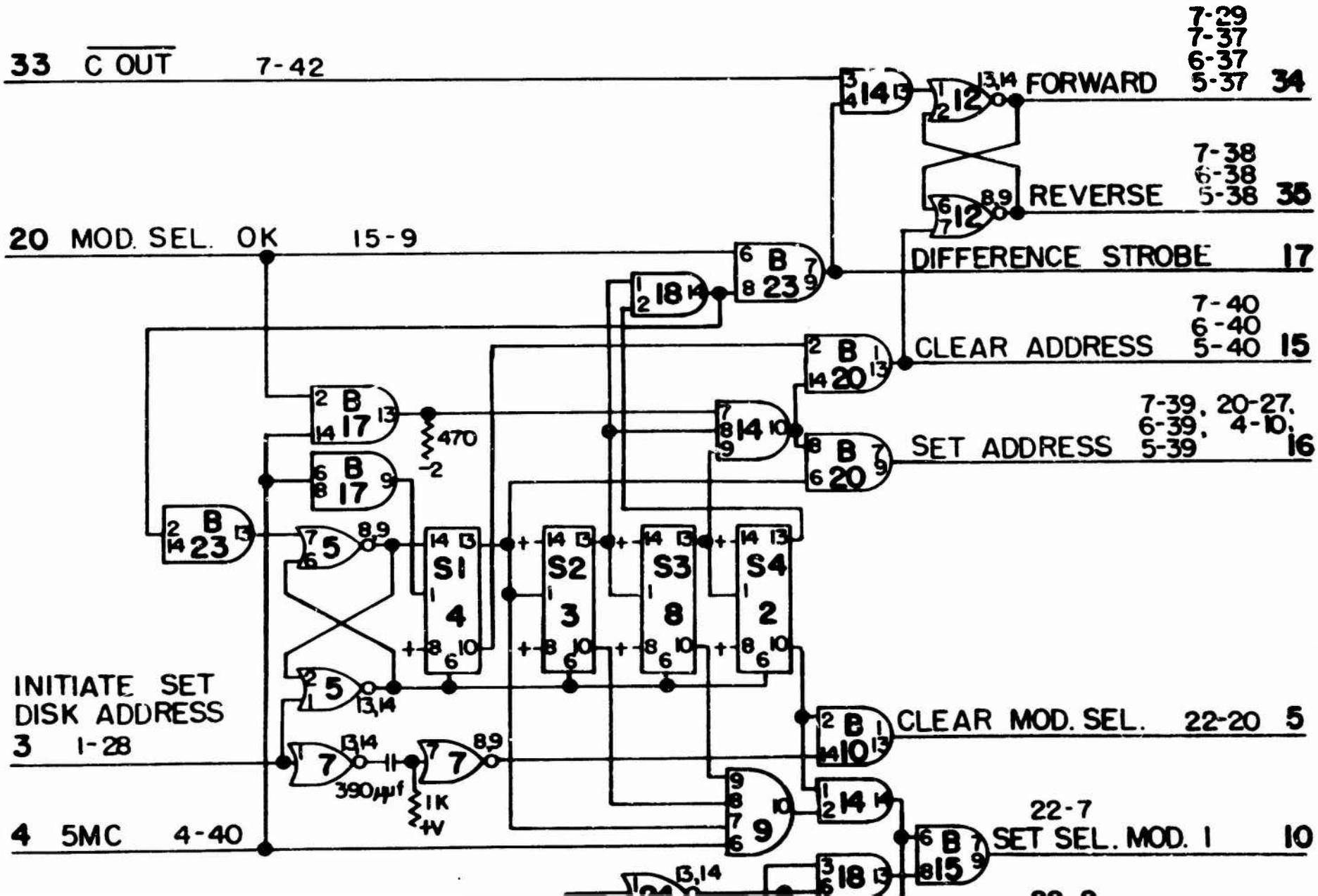
7-16-71

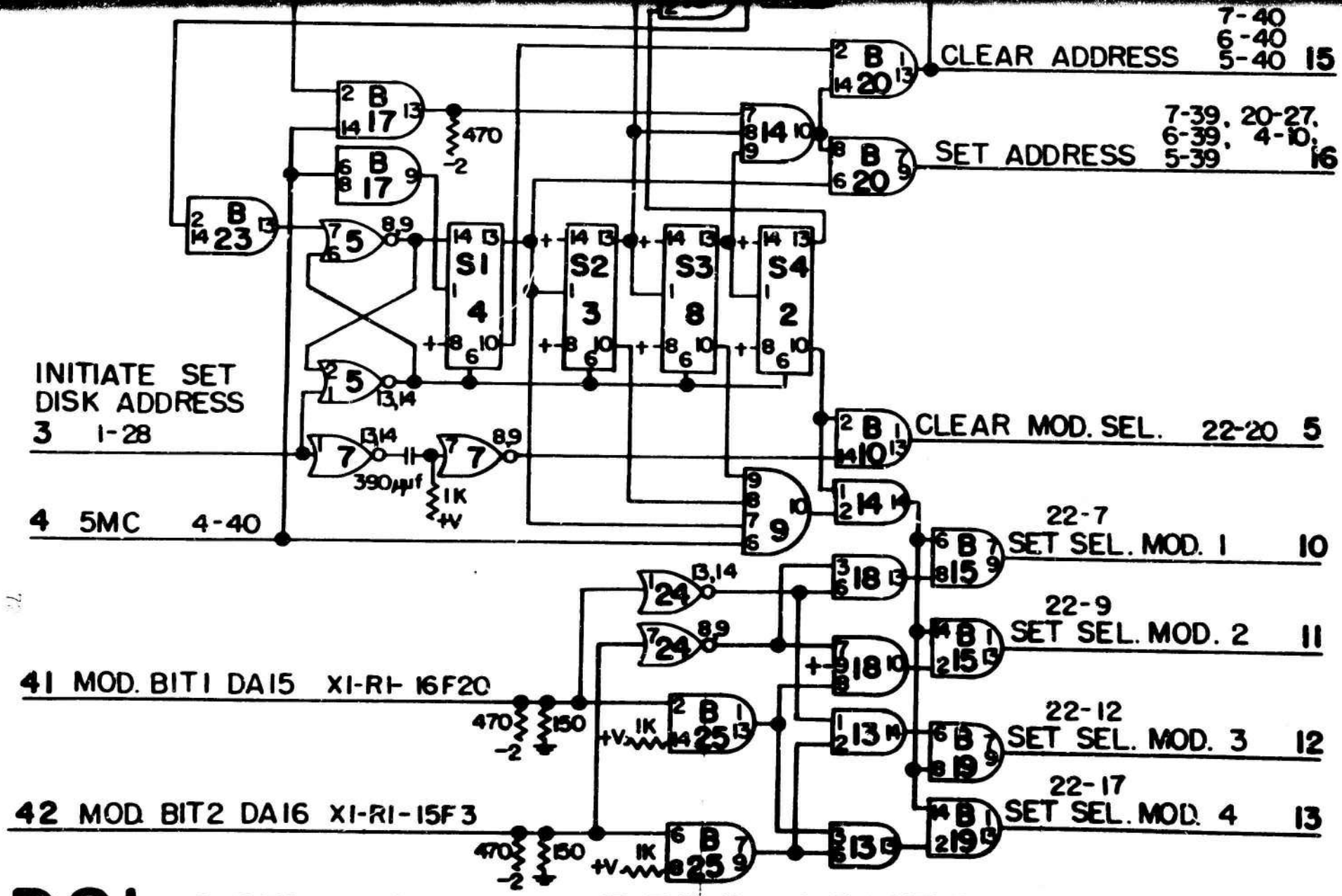

16 GATED ATTENTION U1 23-39
17 GATED ATTENTION U2 23-40
18 GATED ATTENTION U3 23-41
19 GATED ATTENTION U4 23-42
31 U4 SWITCH
32 U3 SWITCH
33 U2 SWITCH
34 U1 SWITCH
11 PRESET 24-8
37 INITIATE READ 1-37
27 SET ADDRESS 21-16
READY 1-20 20
1-41, 22-41
READY PULSE 13
1-9, 22-42
RESET + MACH. +
CONTROLLER CLEAR 42
26 RESET 9-40
25 CRC ERROR 19-25
RELEASE BUFFER (RB) 19-38 1-18 40
+V
1.3K
-2
.6μs



D20 EXCEED CAPACITY COUNTER

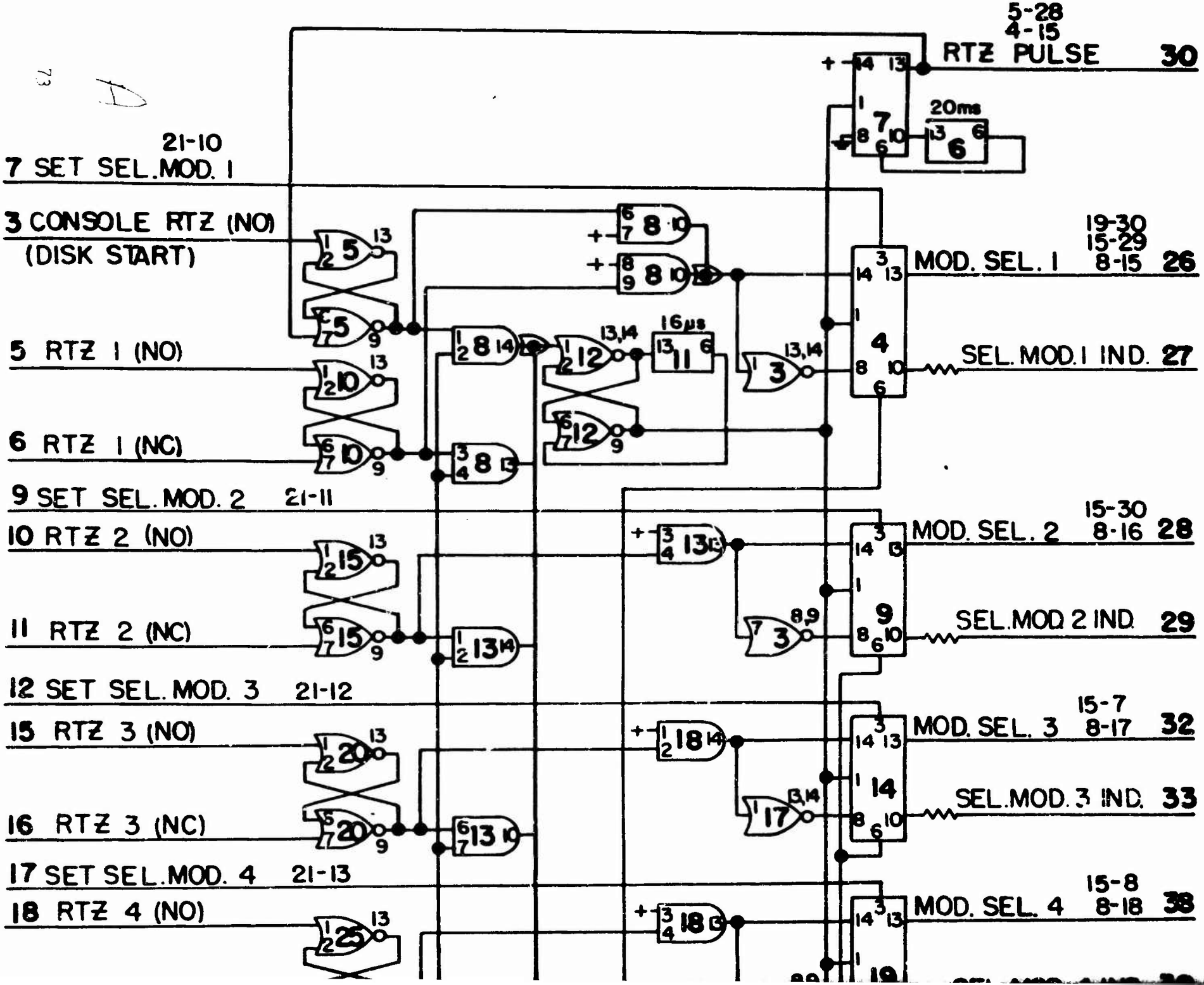
7-16-71

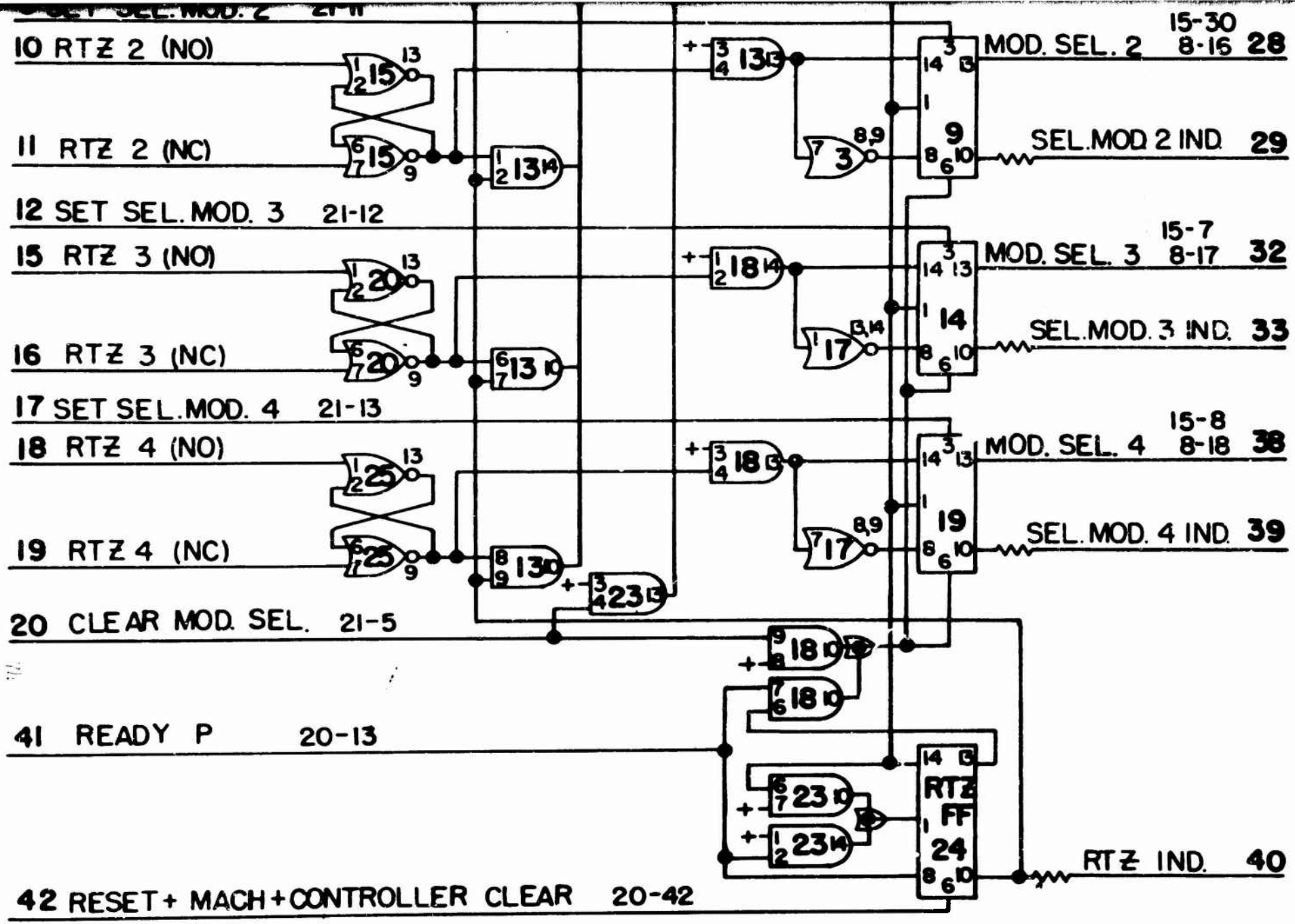

33 C OUT 7-42
20 MOD. SEL. OK 15-9
INITIATE SET DISK ADDRESS
3 1-28
4 5MC 4-40
FORWARD 34
REVERSE 35
DIFFERENCE STROBE 17
CLEAR ADDRESS 15
SET ADDRESS 16
CLEAR MOD. SEL. 22-20 5
SET SEL. MOD. 1 10
7-29
7-37
6-37
5-37
7-38
6-38
5-38
7-40
6-40
5-40
7-39, 20-27,
6-39, 4-10,
5-39
22-7
470
-2
390μμf
1K
+V
S1
4
S2
3
S3
8
S4
2



D21 SET DISK ADDRESS CONTROL

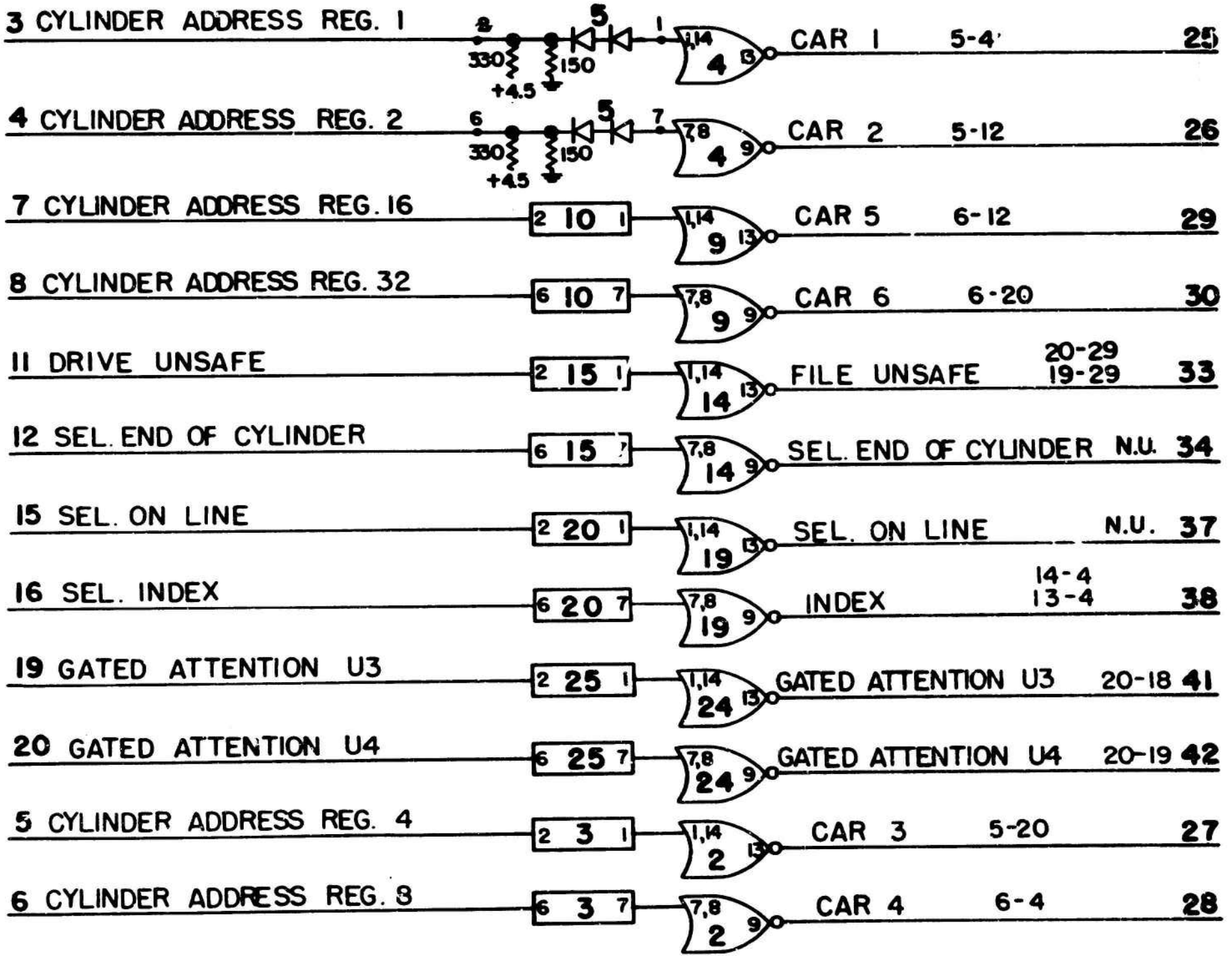
7-16-71

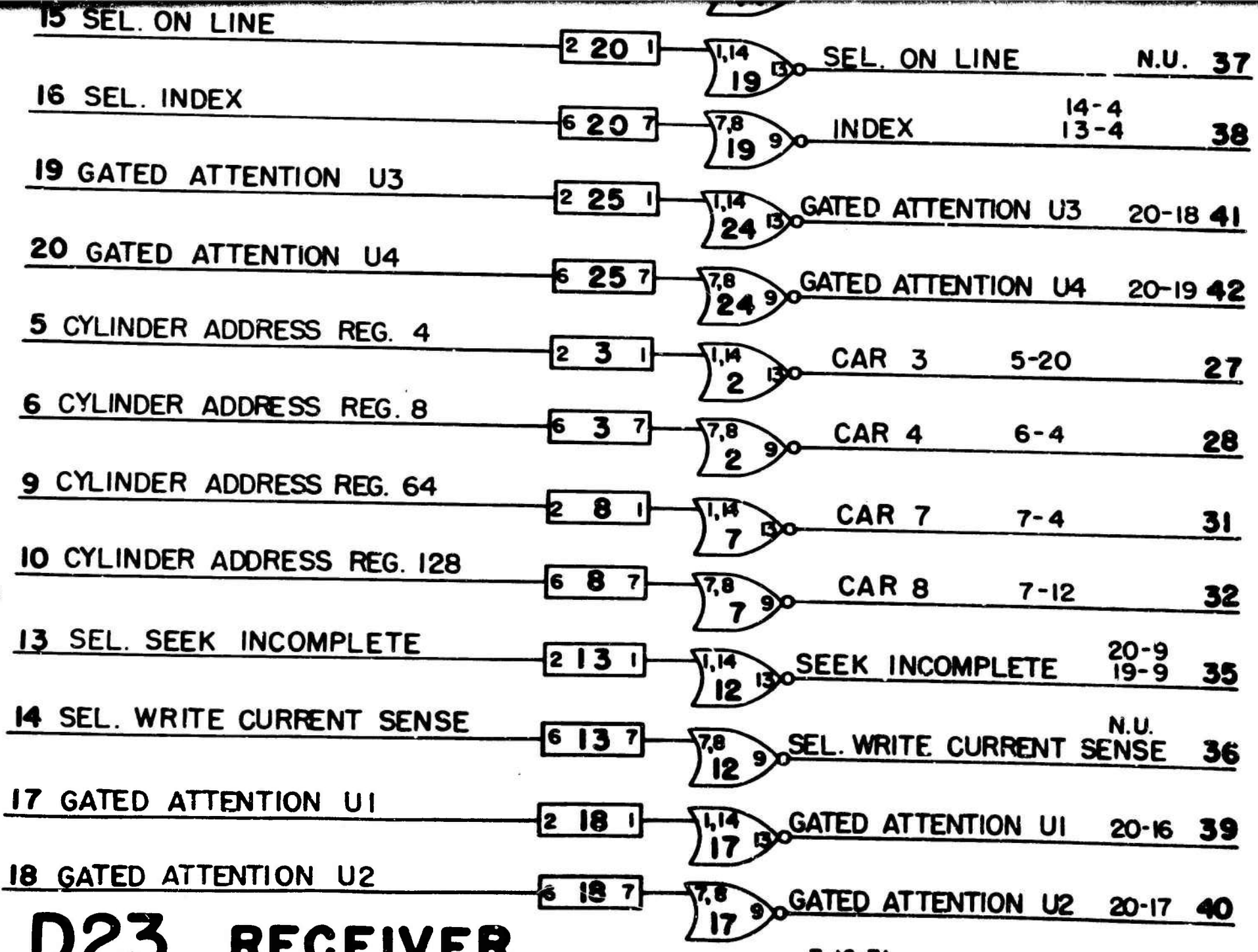

5-28
4-15
RTZ PULSE 30
20ms
21-10
7 SET SEL. MOD. 1
3 CONSOLE RTZ (NO)
(DISK START)
19-30
15-29
MOD. SEL. 1 8-15 26
5 RTZ 1 (NO)
16μs
SEL. MOD. 1 IND. 27
6 RTZ 1 (NC)
9 SET SEL. MOD. 2 21-11
15-30
10 RTZ 2 (NO)
MOD. SEL. 2 8-16 28
11 RTZ 2 (NC)
SEL. MOD. 2 IND. 29
12 SET SEL. MOD. 3 21-12
15-7
15 RTZ 3 (NO)
MOD. SEL. 3 8-17 32
16 RTZ 3 (NC)
SEL. MOD. 3 IND. 33
17 SET SEL. MOD. 4 21-13
15-8
18 RTZ 4 (NO)
MOD. SEL. 4 8-18 38



D22 MOD. SELECT

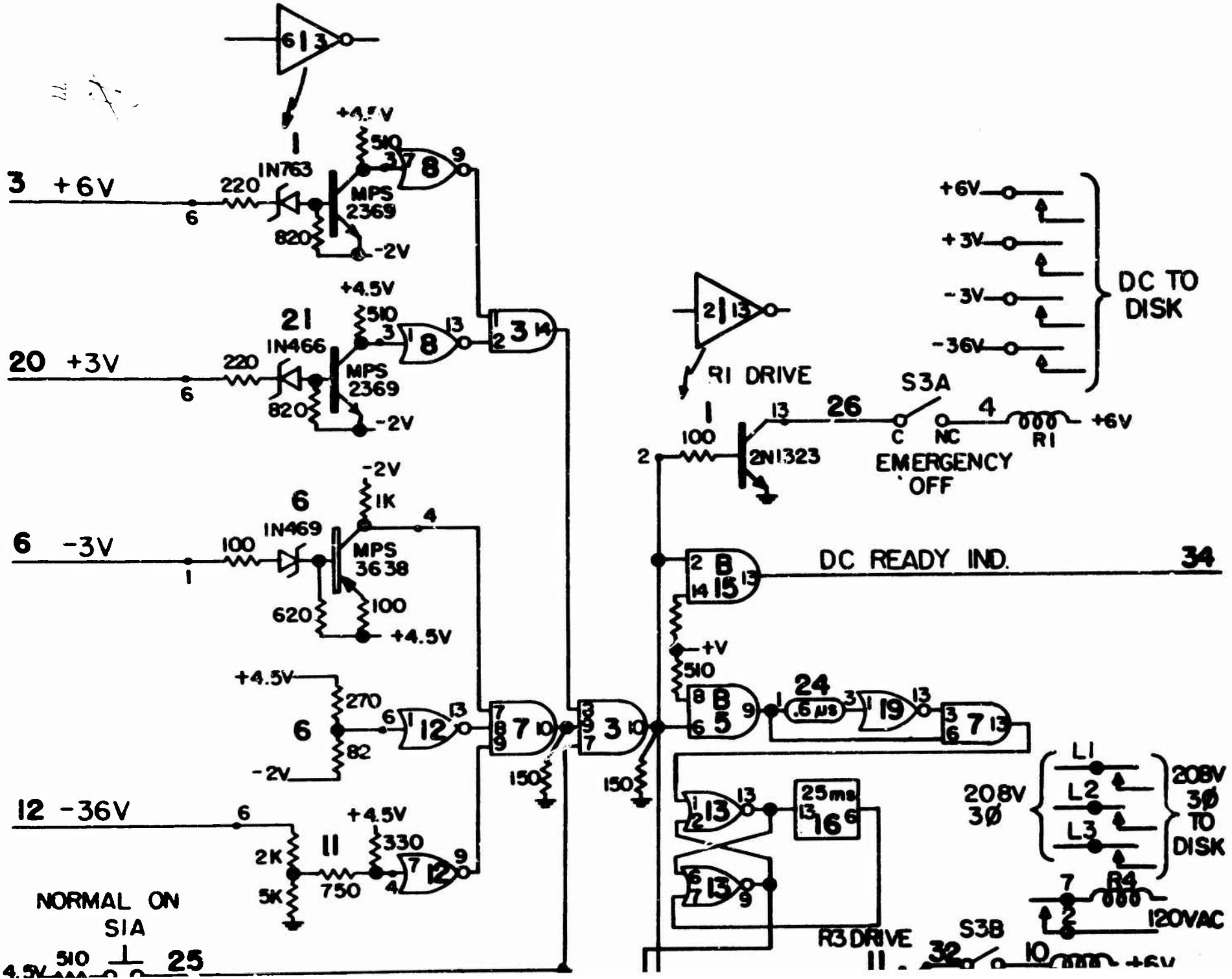
7-16-71


3 CYLINDER ADDRESS REG. 1
8
330
+4.5
150
5
1
1,14
4
13
CAR 1 5-4 25
4 CYLINDER ADDRESS REG. 2
6
330
+4.5
150
5
7
7,8
4
9
CAR 2 5-12 26
7 CYLINDER ADDRESS REG. 16
2 10 1
1,14
9
13
CAR 5 6-12 29
8 CYLINDER ADDRESS REG. 32
6 10 7
7,8
9
9
CAR 6 6-20 30
11 DRIVE UNSAFE
2 15 1
1,14
14
13
FILE UNSAFE 20-29 19-29 33
12 SEL. END OF CYLINDER
6 15 7
7,8
14
9
SEL. END OF CYLINDER N.U. 34
15 SEL. ON LINE
2 20 1
1,14
19
13
SEL. ON LINE N.U. 37
16 SEL. INDEX
6 20 7
7,8
19
9
INDEX 14-4 13-4 38
19 GATED ATTENTION U3
2 25 1
1,14
24
13
GATED ATTENTION U3 20-18 41
20 GATED ATTENTION U4
6 25 7
7,8
24
9
GATED ATTENTION U4 20-19 42
5 CYLINDER ADDRESS REG. 4
2 3 1
1,14
2
13
CAR 3 5-20 27
6 CYLINDER ADDRESS REG. 8
6 3 7
7,8
2
9
CAR 4 6-4 28

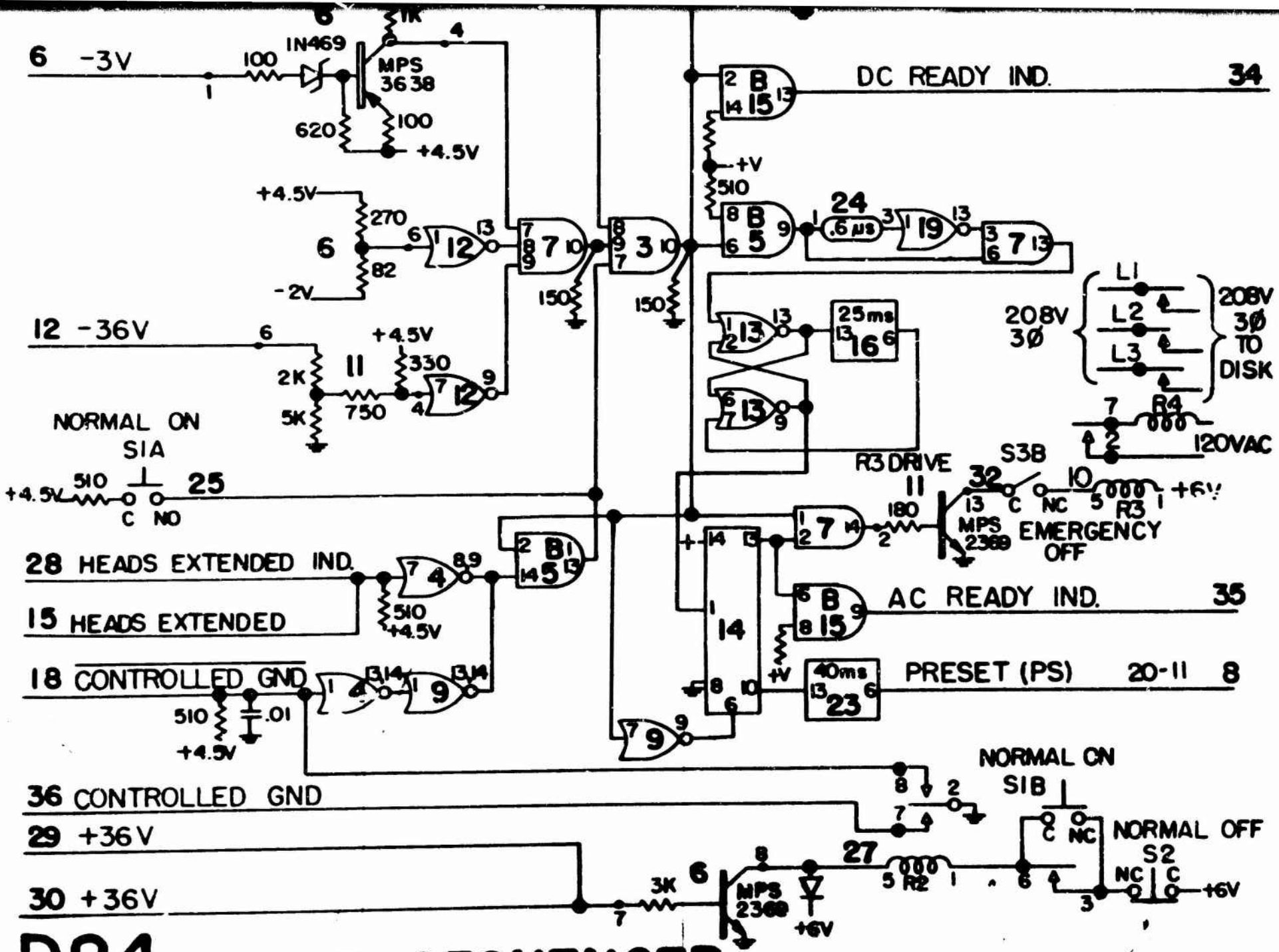


D23 RECEIVER

7-16-71



3 +6V
20 +3V
6 -3V
12 -36V
1N763
1N466
1N469
MPS 2369
MPS 3638
+4.5V
-2V
R1 DRIVE
2N1323
S3A
EMERGENCY OFF
DC TO DISK
DC READY IND.
34
+V
25ms
208V 3Ø
208V 3Ø TO DISK
120VAC
R3 DRIVE
S3B
NORMAL ON S1A


6 -3V
100
IN469
MPS 3638
620
100
+4.5V
1K
+4.5V
270
82
-2V
12 -36V
2K
5K
750
330
NORMAL ON SIA
510
25
C NO
28 HEADS EXTENDED IND.
15 HEADS EXTENDED
510 +4.5V
18 CONTROLLED GND
510
.01
+4.5V
36 CONTROLLED GND
29 +36V
30 +36V
3K
MPS 2369
+6V
DC READY IND. 34
+V
510
24
.6 µs
150
150
25ms
40ms
23
PRESET (PS) 20-11 8
208V 3Ø
208V 3Ø TO DISK
L1
L2
L3
R4
120VAC
R3 DRIVE
S3B
180
MPS 2369
EMERGENCY OFF
AC READY IND. 35
NORMAL ON SIB
NORMAL OFF S2
R2
+6V
D24 POWER SEQUENCER
7-16-71